Figure 15: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

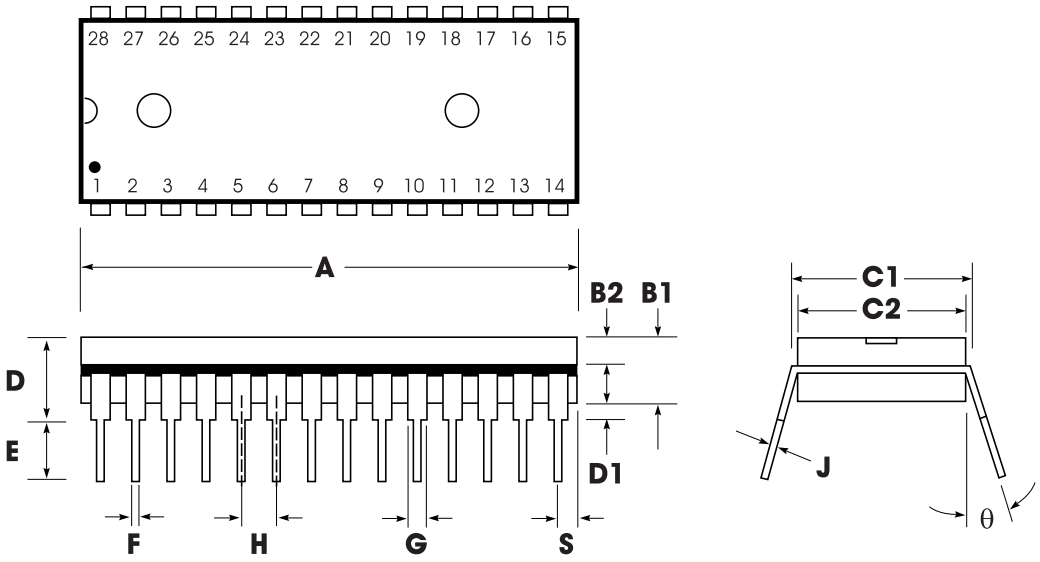


Table 31: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

Figure 16: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

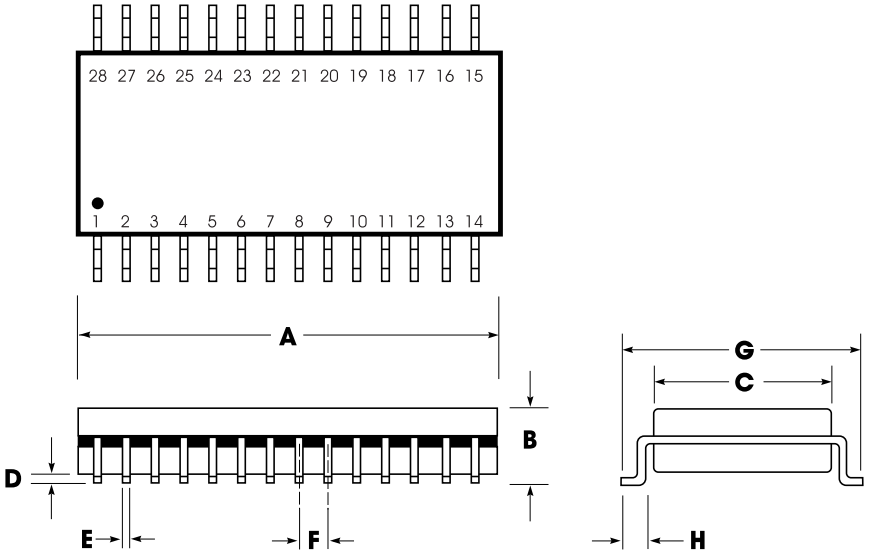


Table 32: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

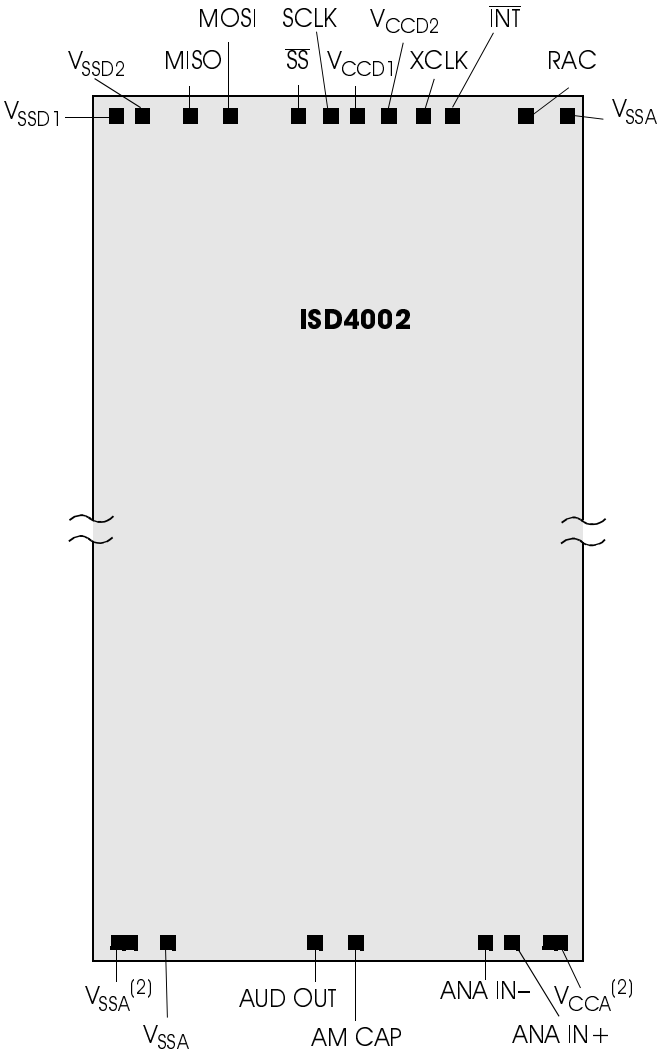
Figure 17: ISD4002 Series Bonding Physical Layout(1) (Unpackaged Die)

ISD4002 Series

I. Die Dimensions
X: 166.6 ±1 mils
Y: 222.5 ±1 mils

II. Die Thickness
11.5 ±0.5 mils(3)

III. Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Double bond recommended.*
3. *This is the current die thickness. Please contact ISD as this thickness may change in the future.*

Table 33: ISD4002 Series Device Pin/Pad Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
V_{SSA}[1]	V_{SS} Analog Power Supply	–1898.1	–2607.4
V_{SSA}	V_{SS} Analog Power Supply	–1599.9	–2607.4
AUD OUT	Audio Output	281.9	–2607.4
AM CAP	AutoMute	577.3	–2607.4
ANA IN –	Inverting Analog Input	1449.3	–2607.4
ANA IN +	Noninverting Analog Input	1603.5	–2607.4
V_{CCA}[1]	V_{CC} Analog Power Supply	1898.7	–2607.4
V_{SSA}	V_{SS} Analog Power Supply	1885.7	2606.7
RAC	Row Address Clock	1483.8	2606.7
$\overline{INT}$	Interrupt	794.8	2606.7
XCLK	External Clock Input	564.8	2606.7
V_{CCD1}	V_{CC} Digital Power Supply	384.9	2606.7
V_{CCD2}	V_{CC} Digital Power Supply	169.5	2606.7
SCLK	Slave Clock	–14.7	2606.7
$\overline{SS}$	Slave Select	–198.1	2606.7
MOSI	Master Out Slave In	–1063.7	2606.7
MISO	Master In Slave Out	–1325.6	2606.7
V_{SSD1}	V_{SS} Digital Power Supply	–1665.3	2606.7
V_{SSD2}	V_{SS} Digital Power Supply	–1836.9	2606.7

1. *Double bond recommended.*

Figure 18: ISD4002 Chip Scale Package (CSP) (Z)

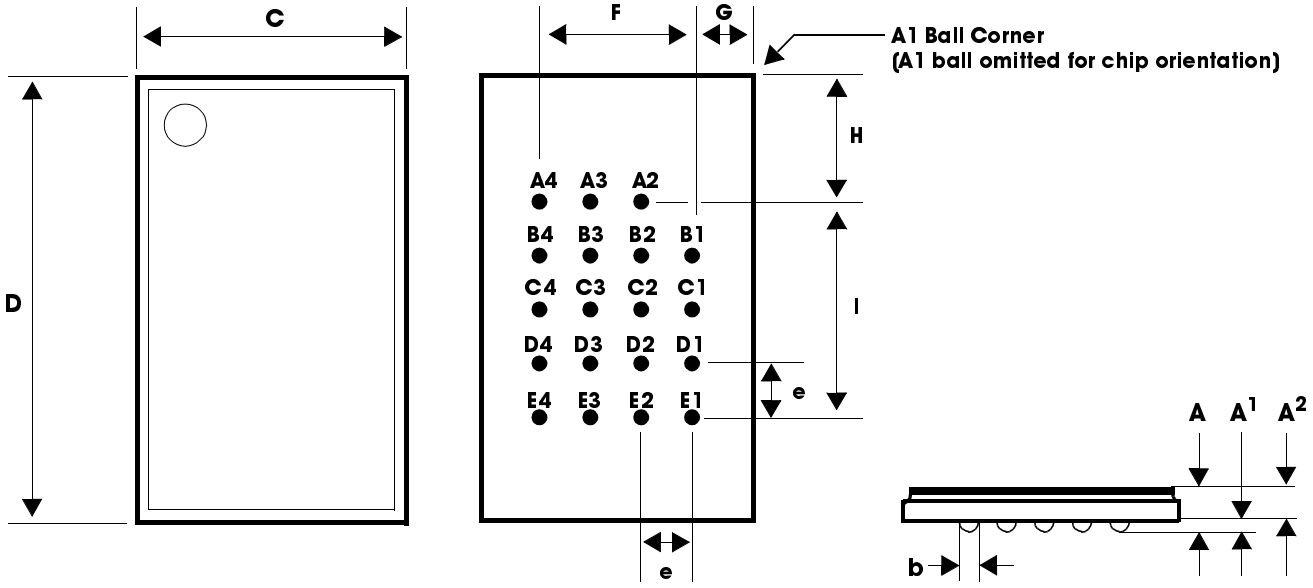


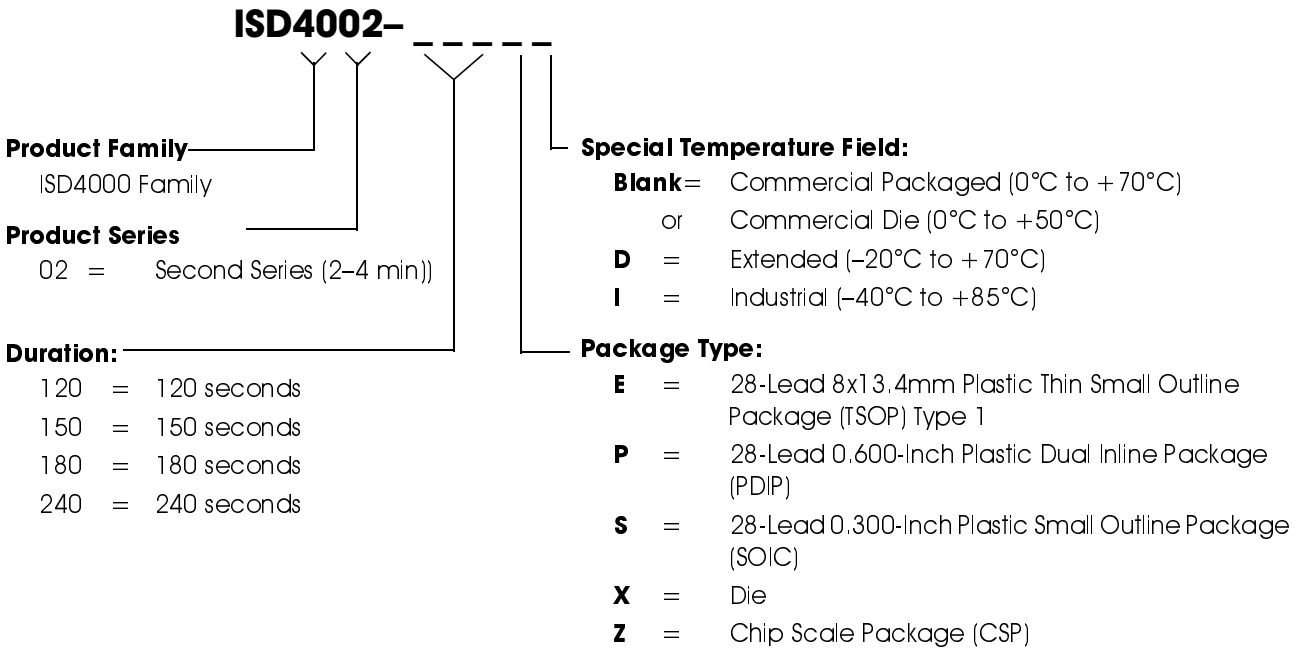
Table 34: CSP Dimensions

Symbol	Min.	Nom.	Max.
A	—	—	0.85
A^1	0.15	—	—
A^2	—	0.55	—
b	0.30	0.35	0.40
C	—	4.70	—
D	—	6.10	—
e		0.75	
F	—	2.25	—
G	—	1.22	—
H	—	1.55	—
I	—	3.00	—

Name	Ball Location	TSOP Pin #
V_{SSA}	A2	18
AM CAP	A3	22
ANAIN+	A4	25
V_{SSA}	B1	17
AUDOUT	B2	20
ANAIN–	B3	24
V_{CCA}	B4	26
V_{SSD1}	C1	12
V_{SSD2}	C2	N/A
V_{CCD2}	C3	N/A
V_{SSA}	C4	1
MOSI	D1	10
SCLK	D2	8
XCLK	D3	6
RAC	D4	2
MISO	E1	11
SS	E2	9
V_{CCD1}	E3	7
INT	E4	5

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD4002 Series devices, please refer to the following valid part numbers.

Part Number	Part Number	Part Number	Part Number
ISD4002-120E	ISD4002-150E	ISD4002-180E	ISD4002-240E
ISD4002-120ED	ISD4002-150ED	ISD4002-180ED	ISD4002-240ED
ISD4002-120EI	ISD4002-150EI	ISD4002-180EI	ISD4002-240EI
ISD4002-120P	ISD4002-150P	ISD4002-180P	ISD4002-240P
ISD4002-120S	ISD4002-150S	ISD4002-180S	ISD4002-240S
ISD4002-120SI	ISD4002-150SI	ISD4002-180SI	ISD4002-240SI
ISD4002-120X	ISD4002-150X	ISD4002-180X	ISD4002-240X
ISD4002-120Z	ISD4002-150Z	ISD4002-180Z	ISD4002-240Z
ISD4002-120ZD	ISD4002-150ZD	ISD4002-180ZD	ISD4002-240ZD
ISD4002-120ZI	ISD4002-150ZI	ISD4002-180ZI	ISD4002-240ZI

For the latest product information, access ISD's worldwide website at http://www.isd.com.