

Table 25: Absolute Maximum Ratings (Die)⁽¹⁾

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V _{SS} – 0.3 V) to (V _{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V _{SS} – 1.0 V) to (V _{CC} + 1.0 V)
Voltage applied to MOSI, SCLK, and SS pins (Input current limited to ±20 mA)	(V _{SS} – 1.0 V) to (V _{CC} + 1.0 V)
V _{CC} – V _{SS}	–0.3 V to +7.0 V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

Table 26: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V _{CC}) ⁽¹⁾	+2.7 V to +3.3 V
Ground voltage (V _{SS}) ⁽²⁾	0 V

1. V_{CC} = V_{CCA} = V_{CCD}

2. V_{SS} = V_{SSA} = V_{SSD}.

Table 27: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			V _{CC} × 0.2	V	
V _{IH}	Input High Voltage	V _{CC} × 0.8			V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 10 μA
V _{OL1}	RAC, INT Output Low Voltage			0.4	V	I _{OL} = 1 mA
V _{OH}	Output High Voltage	V _{CC} – 0.4			V	I _{OH} = –10 μA
I _{CC}	V _{CC} Current (Operating) — Playback — Record		15 25	30 40	mA mA	R _{EXT} = ∞ ⁽³⁾ R _{EXT} = ∞ ⁽³⁾
I _{SB}	V _{CC} Current (Standby)		1	10	μA	⁽³⁾ ⁽⁴⁾
I _{IL}	Input Leakage Current			±1	μA	
I _{HZ}	MISO Tristate Current		1	10	μA	
R _{EXT}	Output Load Impedance	5			KΩ	

Table 27: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
R _{ANA IN+}	ANA IN+ Input Resistance	2.2	3.0	3.8	K Ω	
R _{ANA IN-}	ANA IN- Input Resistance	40	56	71	K Ω	
A _{ARP}	ANA IN+ or ANA IN- to AUDOUT Gain		25		dB	⁽⁵⁾

1. Typical values: $T_A = 25^\circ\text{C}$ and 3.0 V.
2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. V_{CCA} and V_{CCD} connected together.
4. $\overline{SS} = V_{CCA} = V_{CCD}$, $XCLK = MOSI = V_{SSA} = V_{SSD}$ and all other pins floating.
5. Measured with AutoMute feature disabled.

Table 28: AC Parameters (Die)

Symbol	Characteristic		Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD4002-120		8.0		KHz	⁽⁵⁾
		ISD4002-150		6.4		KHz	⁽⁵⁾
		ISD4002-180		5.3		KHz	⁽⁵⁾
		ISD4002-240		4.0		KHz	⁽⁵⁾
F _{CF}	Filter Pass Band	ISD4002-120		3.4		KHz	3dB Roll-Off Point ⁽³⁾ ⁽⁶⁾
		ISD4002-150		2.7		KHz	3dB Roll-Off Point ⁽³⁾ ⁽⁶⁾
		ISD4002-180		2.3		KHz	3dB Roll-Off Point ⁽³⁾ ⁽⁶⁾
		ISD4002-240		1.7		KHz	3dB Roll-Off Point ⁽³⁾ ⁽⁶⁾
T _{REC}	Record Duration	ISD4002-120		120		sec	⁽⁵⁾
		ISD4002-150		150		sec	⁽⁵⁾
		ISD4002-180		180		sec	⁽⁵⁾
		ISD4002-240		240		sec	⁽⁵⁾
T _{PLAY}	Playback Duration	ISD4002-120		120		sec	⁽⁵⁾
		ISD4002-150		150		sec	⁽⁵⁾
		ISD4002-180		180		sec	⁽⁵⁾
		ISD4002-240		240		sec	⁽⁵⁾
T _{PUD}	Power-Up Delay	ISD4002-120		25		msec	
		ISD4002-150		31.25		msec	
		ISD4002-180		37.5		msec	
		ISD4002-240		50		msec	
T _{STOP} or T _{PAUSE}	Stop or Pause in Record or Play	ISD4002-120		50		msec	
		ISD4002-150		62.5		msec	
		ISD4002-180		75		msec	
		ISD4002-240		100		msec	

Table 28: AC Parameters (Die)

Symbol	Characteristic		Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T_{RAC}	RAC Clock Period	ISD4002-1 20		200		msec	
		ISD4002-1 50		250		msec	
		ISD4002-1 80		300		msec	
		ISD4002-240		400		msec	
T_{RACLO}	RAC Clock Low Time	ISD4002-1 20		25		msec	(9)
		ISD4002-1 50		31.25		msec	(9)
		ISD4002-1 80		37.5		msec	(9)
		ISD4002-240		50		msec	(9)
T_{RACM}	RAC Clock Period in Message Cueing Mode	ISD4002-1 20		125		μ sec	
		ISD4002-1 50		156.3		μ sec	
		ISD4002-1 80		187.5		μ sec	
		ISD4002-240		250		μ sec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD4002-1 20		15.63		μ sec	
		ISD4002-1 50		19.53		μ sec	
		ISD4002-1 80		23.44		μ sec	
		ISD4002-240		31.25		μ sec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak ⁽⁴⁾ (7) (8)

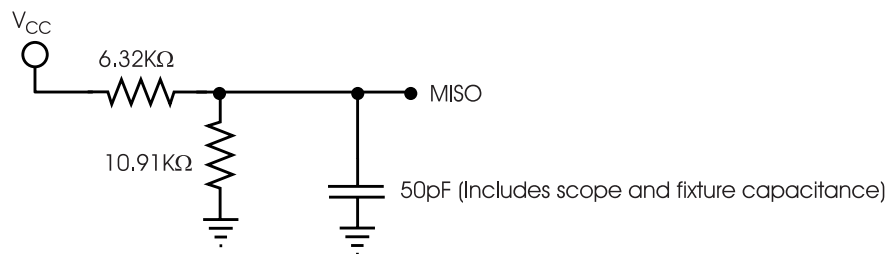
1. Typical values: $T_A = 25^\circ\text{C}$ and 3.0 V.
2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).
4. Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN- is 16 mV peak-to-peak.
5. Sampling Frequency and Duration can vary as much as ± 2.25 percent over the commercial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Filter specification applies to the anti-aliasing filter and to the smoothing filter.
7. The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.
8. For optimal signal quality, this maximum limit is recommended.
9. When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.

Table 29: SPI AC Parameters⁽¹⁾

Symbol	Characteristics	Min	Max	Units	Conditions
T_{SS}	$\overline{SS}$ Setup Time	500		nsec	
T_{SSH}	$\overline{SS}$ Hold Time	500		nsec	
T_{DIS}	Data in Setup Time	200		nsec	
T_{DIH}	Data in Hold Time	200		nsec	
T_{PD}	Output Delay		500	nsec	
$T_{DF}^{(2)}$	Output Delay to hiZ		500	nsec	
T_{SSmin}	$\overline{SS}$ HIGH	1		μ sec	
T_{SCKhi}	SCLK High Time	400		nsec	
T_{SCKlow}	SCLK Low Time	400		nsec	
F_0	CLK Frequency		1,000	KHz	

1. Typical values: $T_A = 25^\circ\text{C}$ and 3.0 V. Timing measured at 50 percent of the V_{CC} level.

2. Tristate test condition.



TIMING DIAGRAMS

Figure 6: Timing Diagram

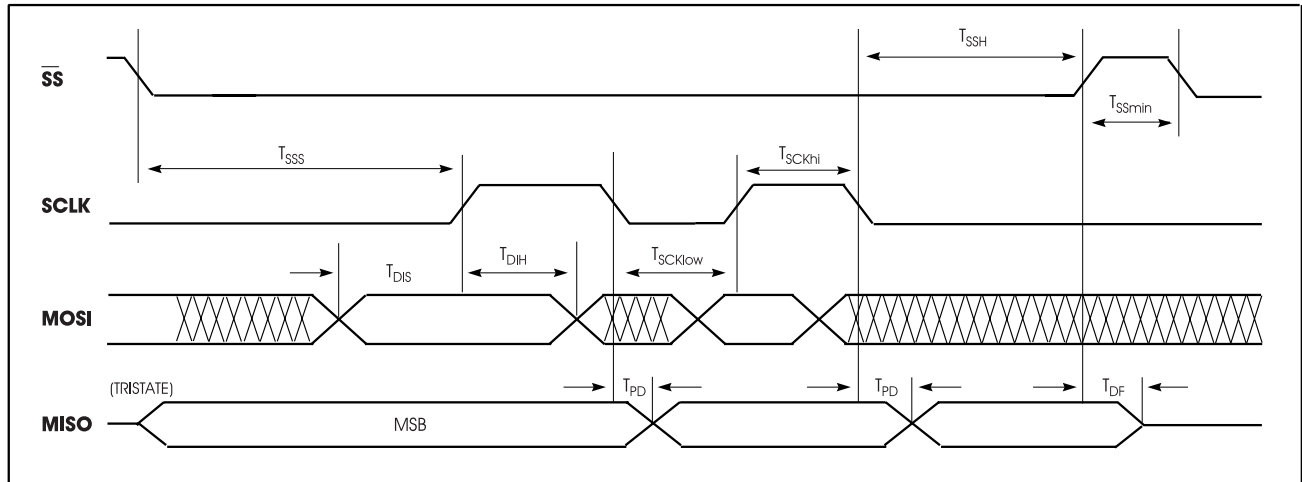


Figure 7: 8-Bit Command Format

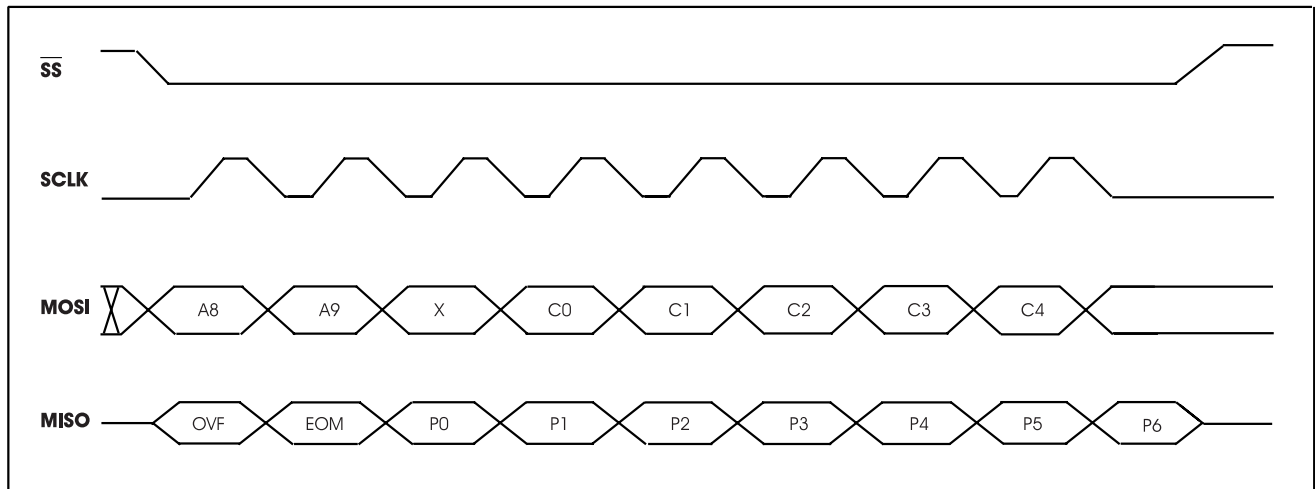


Figure 8: 16-Bit Command Format

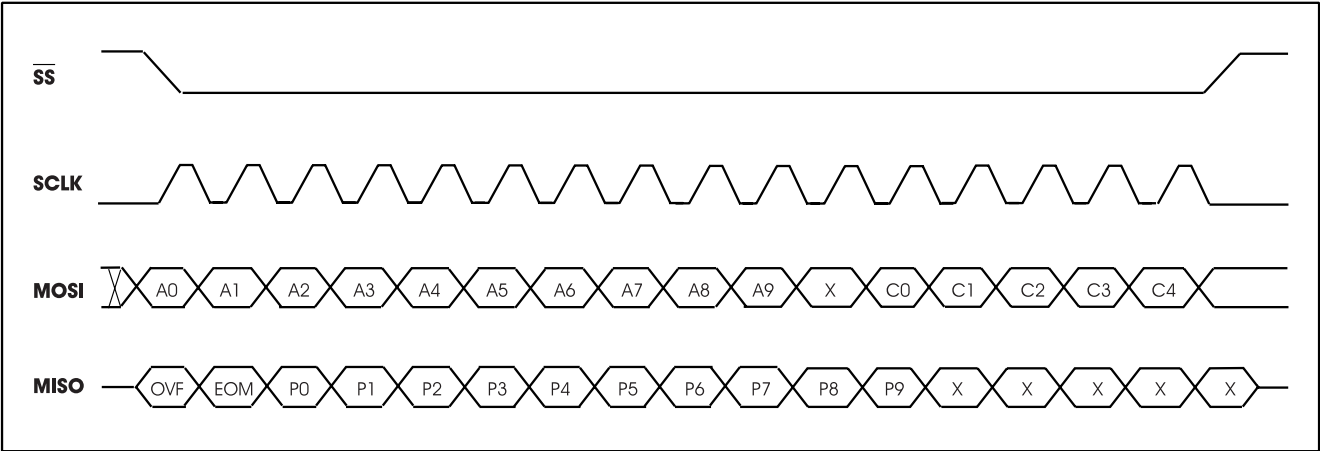


Figure 9: Playback/Record and Stop Cycle

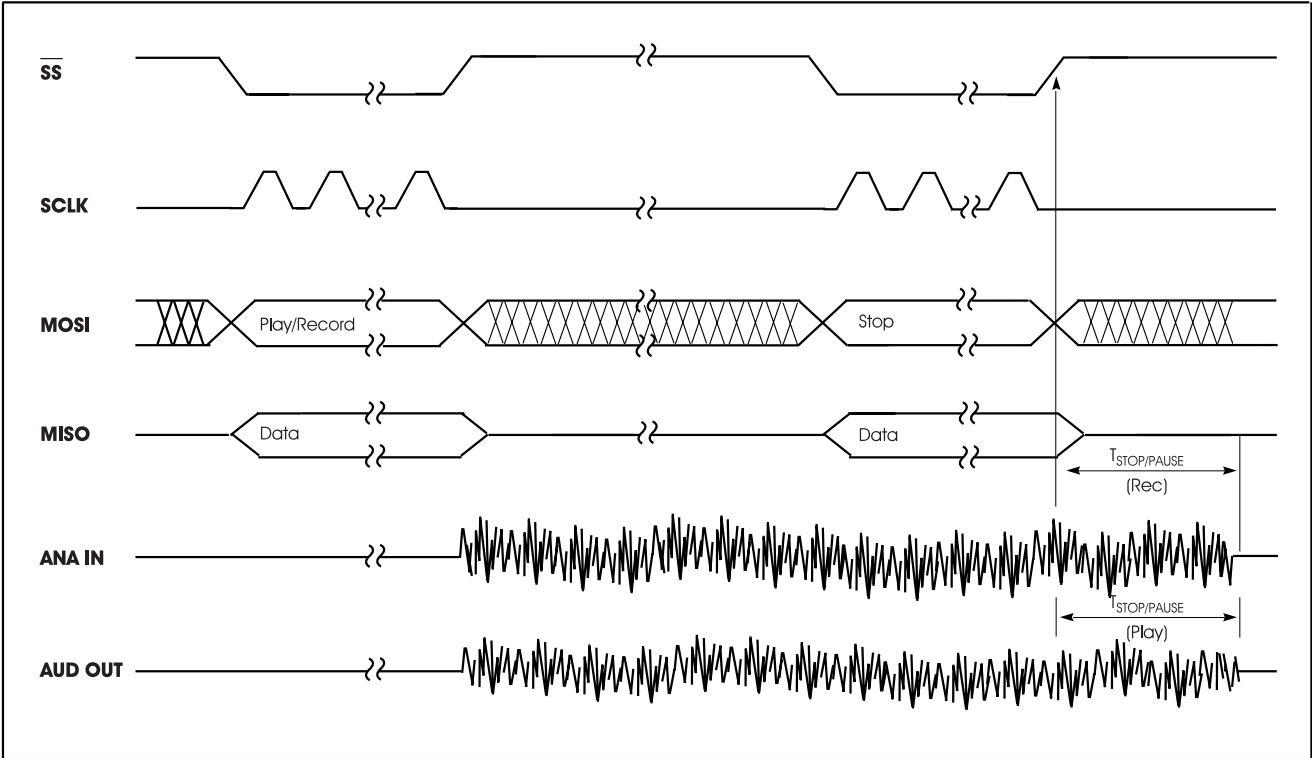
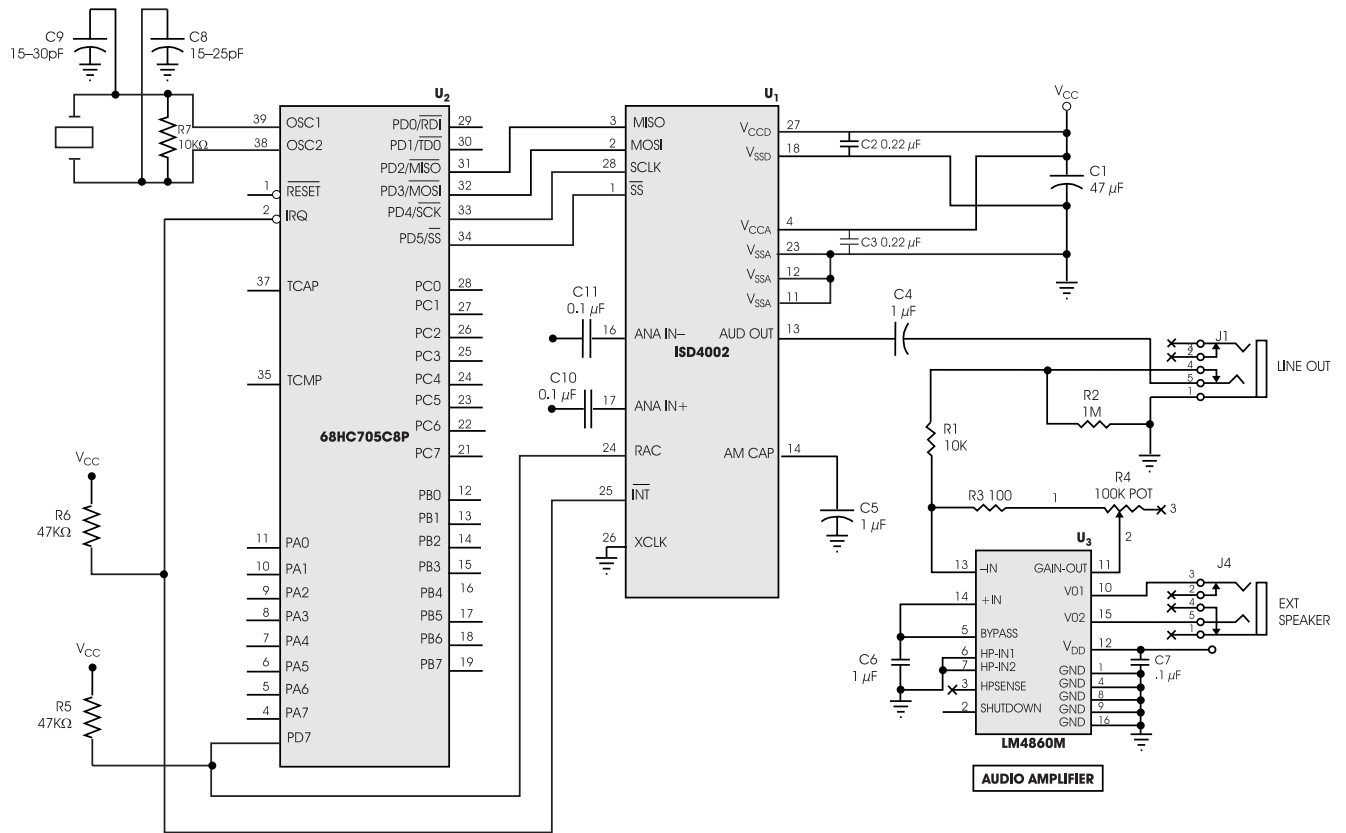
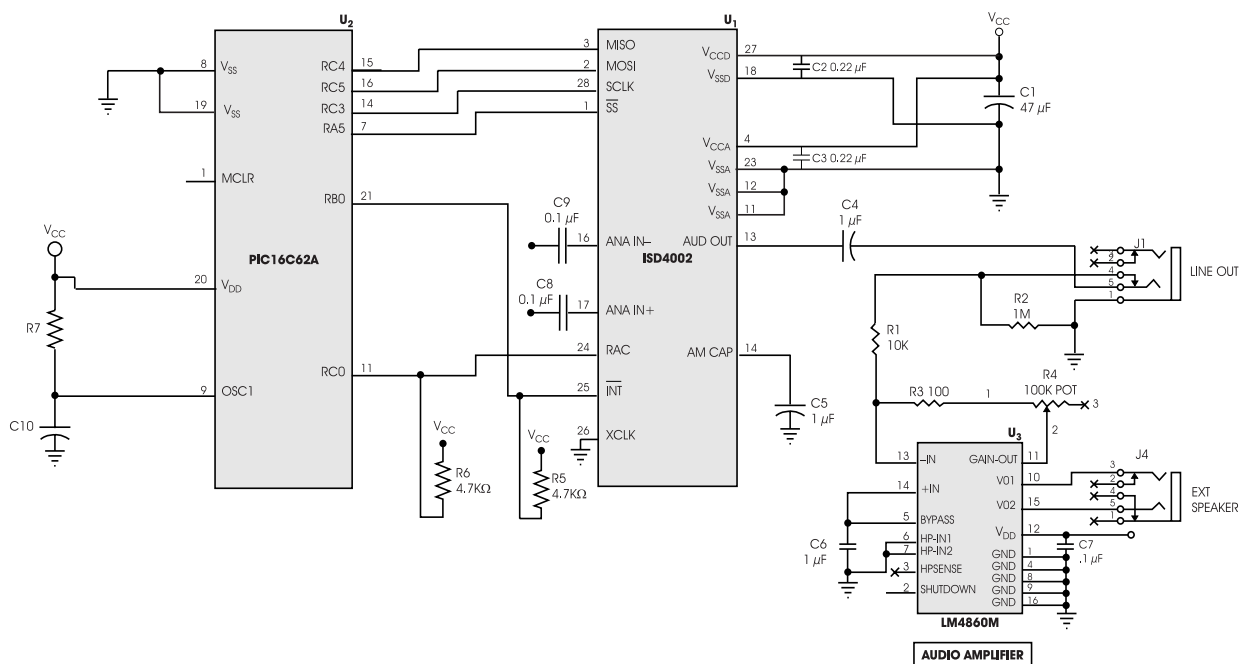
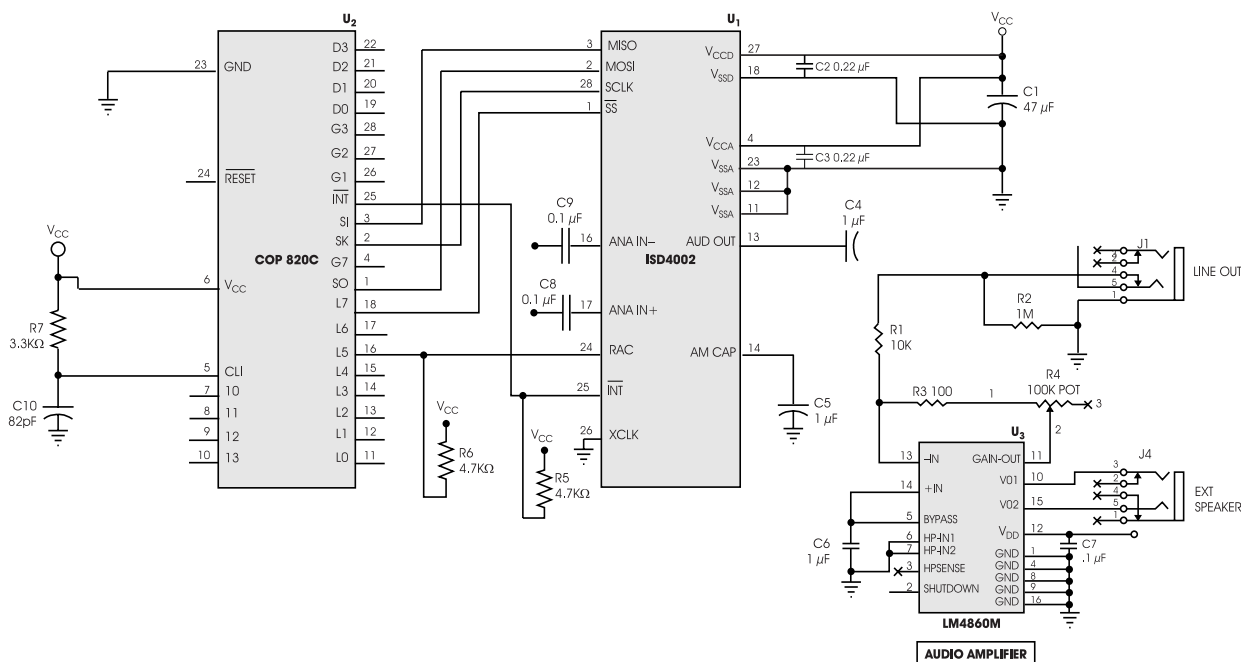


Figure 10: Application Example Using SPI⁽¹⁾

1. This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.
2. Please make sure the bypass capacitor C2 is as close as possible to the package.

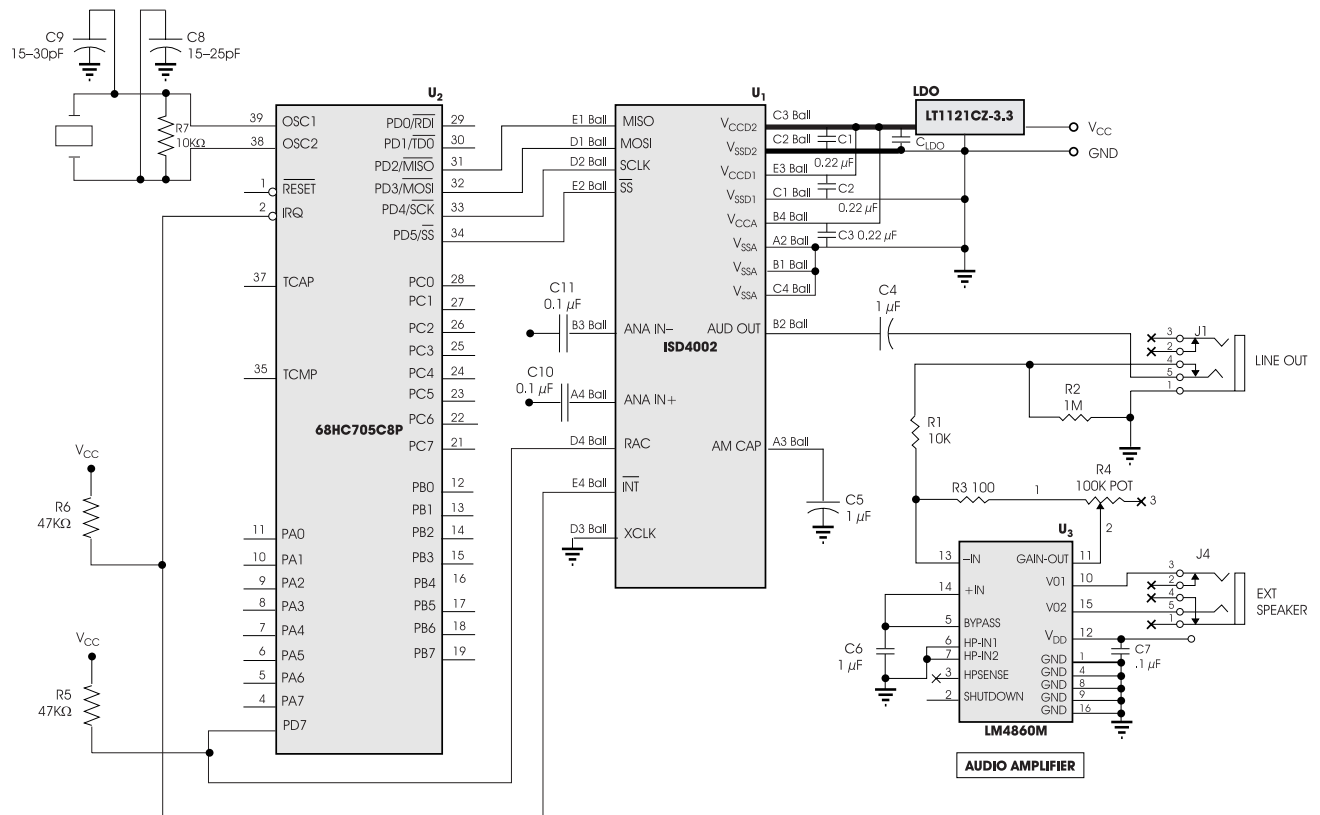
Figure 11: Application Example Using Microwire⁽¹⁾

1. This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.
2. Please make sure the bypass capacitor C2 is as close as possible to the package.

Figure 12: Application Example Using SPI Port on Microcontroller⁽¹⁾

1. This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.
2. Please make sure the bypass capacitor C2 is as close as possible to the package.

Figure 13: Application Example Using SPI with a Chip Scale Packaged Device



1. This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.
2. Please make sure all bypass capacitors are as close as possible to the package.
3. Ground plane must be used to connect all V_{SSA} pins together. If a ground plane is not available then a short and low impedance path is necessary.
4. Route ANA IN+ and ANA IN- away from V_{CCD} and V_{SSD} return paths.
5. Biasing for electret microphone must come from V_{CCA} and V_{SSA}.
6. AM CAP must return to V_{SSA}.
7. Traces from V_{CCD2} to the LDO (Low Dropout regulator) and from V_{SSD2} to the LDO ground should be as thick as possible. The distance between these two traces should be as short as possible.

DEVICE PHYSICAL DIMENSIONS

Figure 14: 28-Lead 8x13.4 mm Plastic Thin Small Outline Package (TSOP) Type I (E)

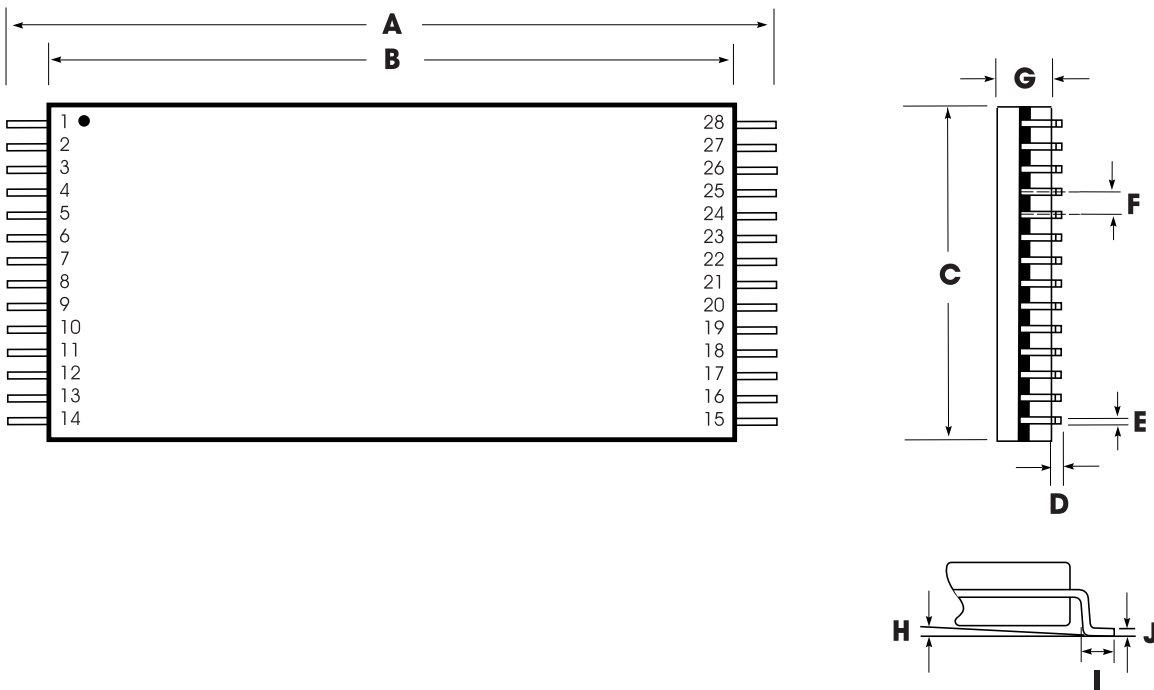


Table 30: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: Lead coplanarity to be within 0.004 inches.