Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ[1]	Max[2]	Units	Conditions
T_{REC}	Record Duration	ISD33060	57.4		62.3	sec	Commercial[6]
		ISD33060D	57.4		62.9	sec	Extended[6]
		ISD33060I	55.9		64.8	sec	Industrial[6]
		ISD33075	71.8		77.8	sec	Commercial[6]
		ISD33075D	71.8		78.6	sec	Extended[6]
		ISD33075I	69.9		81.0	sec	Industrial[6]
		ISD33090	86.2		93.4	sec	Commercial[6]
		ISD33090D	86.2		94.3	sec	Extended[6]
		ISD33090I	83.9		97.3	sec	Industrial[6]
		ISD33120-4	114.9		124.5	sec	Commercial[6]
		ISD33120-4D	114.9		125.7	sec	Extended[6]
		ISD33120-4I	111.8		129.7	sec	Industrial[6]
T_{PLAY}	Playback Duration	ISD33060	57.4		62.3	sec	Commercial[6]
		ISD33060D	57.4		62.9	sec	Extended[6]
		ISD33060I	55.9		64.8	sec	Industrial[6]
		ISD33075	71.8		77.8	sec	Commercial[6]
		ISD33075D	71.8		78.6	sec	Extended[6]
		ISD33075I	69.9		81.0	sec	Industrial[6]
		ISD33090	86.2		93.4	sec	Commercial[6]
		ISD33090D	86.2		94.3	sec	Extended[6]
		ISD33090I	83.9		97.3	sec	Industrial[6]
		ISD33120-4	114.9		124.5	sec	Commercial[6]
		ISD33120-4D	114.9		125.7	sec	Extended[6]
		ISD33120-4I	111.8		129.7	sec	Industrial[6]
T_{PUD}	Power-Up Delay	ISD33060	23.9		26.0	msec	Commercial[6]
		ISD33060D	23.9		26.2	msec	Extended[6]
		ISD33060I	23.3		27.0	msec	Industrial[6]
		ISD33075	29.9		32.4	msec	Commercial[6]
		ISD33075D	29.9		32.7	msec	Extended[6]
		ISD33075I	29.1		33.8	msec	Industrial[6]
		ISD33090	35.9		38.9	msec	Commercial[6]
		ISD33090D	35.9		39.3	msec	Extended[6]
		ISD33090I	34.9		40.5	msec	Industrial[6]
		ISD33120-4	47.9		51.9	msec	Commercial[6]
		ISD33120-4D	47.9		52.4	msec	Extended[6]
		ISD33120-4I	46.6		54.0	msec	Industrial[6]
T_{STOP} or T_{PAUSE}	Stop or Pause in Record or Play	ISD33060		25.0		msec	
		ISD33075		31.25		msec	
		ISD33090		37.5		msec	
		ISD33120-4		50.0		msec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ(1)	Max(2)	Units	Conditions
T_{RAC}	RAC Clock Period	ISD33060	143.7		155.6	msec	Commercial(6) (10)
		ISD33060D	143.7		157.1	msec	Extended(6) (10)
		ISD33060I	139.8		162.0	msec	Industrial(6) (10)
		ISD33075	179.6		194.5	msec	Commercial(6) (10)
		ISD33075D	179.6		196.3	msec	Extended(6) (10)
		ISD33075I	174.7		202.6	msec	Industrial(6) (10)
		ISD33090	215.5		233.3	msec	Commercial(6) (10)
		ISD33090D	215.5		235.6	msec	Extended(6) (10)
		ISD33090I	209.7		243.1	msec	Industrial(6) (10)
		ISD33120-4	287.3		311.1	msec	Commercial(6) (10)
		ISD33120-4D	287.3		314.1	msec	Extended(6) (10)
		ISD33120-4I	279.6		324.1	msec	Industrial(6) (10)
T_{RACLO}	RAC Clock Low Time	ISD33060	11.9		13.0	msec	Commercial(6)
		ISD33060D	11.9		13.1	msec	Extended(6)
		ISD33060I	11.6		13.5	msec	Industrial(6)
		ISD33075	14.9		16.2	msec	Commercial(6)
		ISD33075D	14.9		16.4	msec	Extended(6)
		ISD33075I	14.5		16.9	msec	Industrial(6)
		ISD33090	17.9		19.5	msec	Commercial(6)
		ISD33090D	17.9		19.7	msec	Extended(6)
		ISD33090I	17.4		20.3	msec	Industrial(6)
		ISD33120-4	23.9		26.0	msec	Commercial(6)
		ISD33120-4D	23.9		26.2	msec	Extended(6)
		ISD33120-4I	23.3		27.0	msec	Industrial(6)
T_{RACM}	RAC Clock Period Message in Cueing Mode	ISD33060		187.50		µsec	
		ISD33075		234.40		µsec	
		ISD33090		281.25		µsec	
		ISD33120-4		375.00		µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD33060		15.62		µsec	
		ISD33075		19.56		µsec	
		ISD33090		23.42		µsec	
		ISD33120-4		31.24		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak(4) (8) (9)

1. *Typical values @ T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, V_{IN} max. for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*
5. *For greater stability, an external clock can be utilized, see "ISD33000 Series Pinouts" on page 2.*
6. *Minimum and maximum limits are guaranteed by ISD via 100 percent electrical testing or characterization to meet or exceed a Cpk of 1.33.*
7. *Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.*
8. *The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.*
9. *For optimal signal quality, this maximum limit is recommended.*
10. *When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.*

Table 8: Absolute Maximum Ratings (Die)

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} –0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
Voltage applied to MOSI, SCLK, and SS pins (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to 5.5 V
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+2.7 V to +3.3 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8		3.3[3]	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 µA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current (Operating) Playback Record		 25 30	 30 40	 mA mA	 $R_{EXT} = \infty$ [4] $R_{EXT} = \infty$ [4]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[4] [5]
I_{IL}	Input Leakage Current			±1	µA	
I_{HZ}	MISO Tristate Current		1	10	µA	
R_{EXT}	Output Load Impedance	5			KΩ	

Table 10: DC Parameters (Die)

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Units	Conditions
$R_{ANA\ IN+}$	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
$R_{ANA\ IN-}$	ANA IN– Input Resistance	40	56	71	KΩ	
A_{ARP}	ANA IN+ or ANA IN- to AUDOUT Gain		25		dB	(5)

1. *Typical values @ T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *When driven by a 5-volt microcontroller, the maximum V_{IH} for the MOSI, SCLK, and $\overline{SS}$ pins is 5.5 volts.*
4. *V_{CCA} and V_{CCD} connected together.*
5. *$\overline{SS}$ = V_{CCA}= V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSD} and all other pins floating.*
6. *Measured with AutoMute feature disabled.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD33060		8.0		KHz	(5)
		ISD33075		6.4		KHz	(5)
		ISD33090		5.3		KHz	(5)
		ISD33120-4		4.0		KHz	(5)
F_{CF}	Filter Pass Band	ISD33060		3.4		KHz	3dB Roll-Off Point (3)(7)
		ISD33075		2.7		KHz	3dB Roll-Off Point (3)(7)
		ISD33090		2.3		KHz	3dB Roll-Off Point (3)(7)
		ISD33120-4		1.7		KHz	3dB Roll-Off Point (3)(7)
T_{REC}	Record Duration	ISD33060	57.7		62.7	sec	(5) (6)
		ISD33075	72.1		78.3	sec	(5) (6)
		ISD33090	86.5		94.0	sec	(5) (6)
		ISD33120-4	115.6		126	sec	(5) (6)
T_{PLAY}	Playback Duration	ISD33060	57.7		62.7	sec	(5) (6)
		ISD33075	72.1		78.3	sec	(5) (6)
		ISD33090	86.5		94.0	sec	(5) (6)
		ISD33120-4	115.6		126.0	sec	(5) (6)
T_{PUD}	Power-Up Delay	ISD33060	24.0		26.1	msec	(6
		ISD33075	30.0		32.7	msec	(6)
		ISD33090	36.0		39.2	msec	(6)
		ISD33120-4	48.1		52.5	msec	(6))
T_{STOP} or T_{PAUSE}	Stop or Pause in Record or Play	ISD33060		25.0		msec	
		ISD33075		31.25		msec	
		ISD33090		37.5		msec	
		ISD33120-4		50.0		msec	
T_{RAC}	RAC Clock Period	ISD33060	144.0		156.6	msec	(6) (10)
		ISD33075	180.0		195.8	msec	(6) (10)
		ISD33090	216.0		234.9	msec	(6) (10)
		ISD33120-4	288.9		314.8	msec	(6) (10)

Table 11: AC Parameters (Die)

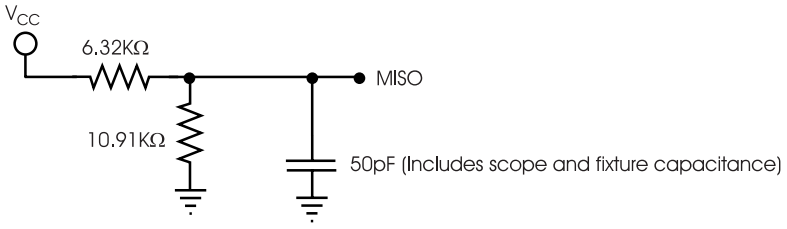
Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{RACLO}	RAC Clock Low Time	ISD33060		12.5		msec	[6]
		ISD33075		15.63		msec	[6]
		ISD33090		18.75		msec	[6]
		ISD33120-4		25.0		msec	[6]
T_{RACM}	RAC Clock Period in Message Cueing Mode	ISD33060		187.5		µsec	
		ISD33075		233.75		µsec	
		ISD33090		281.25		µsec	
		ISD33120-4		375.0		µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD33060		15.62		µsec	
		ISD33075		19.56		µsec	
		ISD33090		23.42		µsec	
		ISD33120-4		31.24		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak[4][8] [9]

1. *Typical values @ T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, V_{IN} max. for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*
5. *For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Minimum and maximum limits are guaranteed by ISD via 100 percent electrical testing or characterization to meet or exceed a Cpk of 1.33.*
7. *Filter specification applies to the antialiasing filter and to the smoothing filter.*
8. *The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.*
9. *For optimal signal quality, this maximum limit is recommended.*
10. *When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.*

Table 12: SPI AC Parameters(1)

Symbol	Characteristics	Min	Max	Units	Conditions
T_{SSS}	$\overline{SS}$ Setup Time	500		nsec	
T_{SSH}	$\overline{SS}$ Hold Time	500		nsec	
T_{DIS}	Data in Setup Time	200		nsec	
T_{DIH}	Data in Hold Time	200		nsec	
T_{PD}	Output Delay		500	nsec	
T_{DF}(2)	Output Delay to hiZ		500	nsec	
T_{SSmin}	$\overline{SS}$ HIGH	1		µsec	
T_{SCKhi}	SCLK High Time	400		nsec	
T_{SCKlow}	SCLK Low Time	400		nsec	
F_0	CLK Frequency		1,000	KHz	

1. *Typical values @T_A = 25°C and 3.0 V. Timing measured at 50 percent of the V_{CC} level.*
2. *Tristate test condition.*



TIMING DIAGRAMS

Figure 5: Timing Diagram

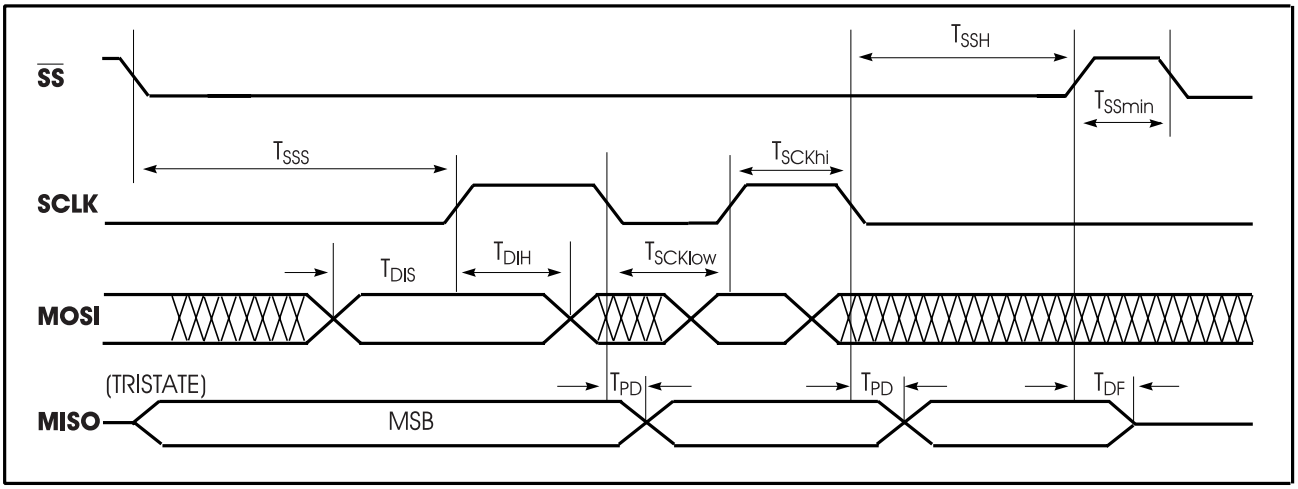


Figure 6: 8-Bit Command Format

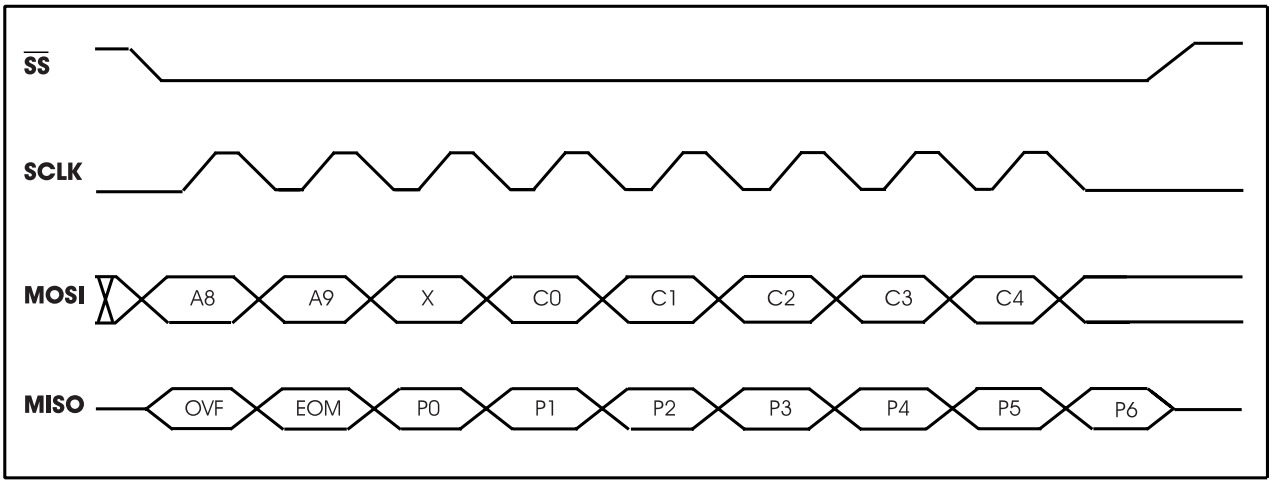


Figure 7: 16-Bit Command Format

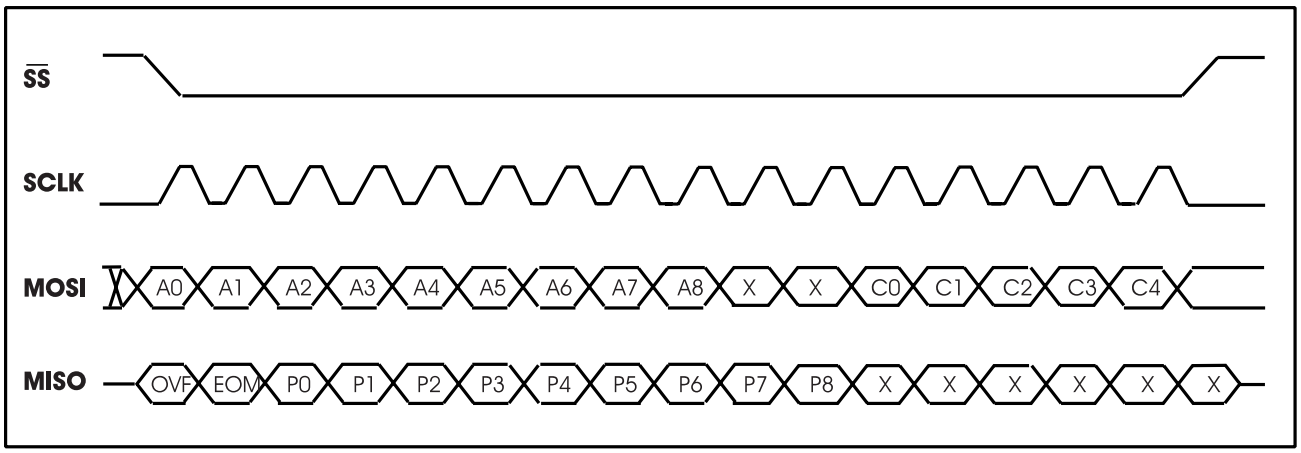


Figure 8: Playback/Record and Stop Cycle

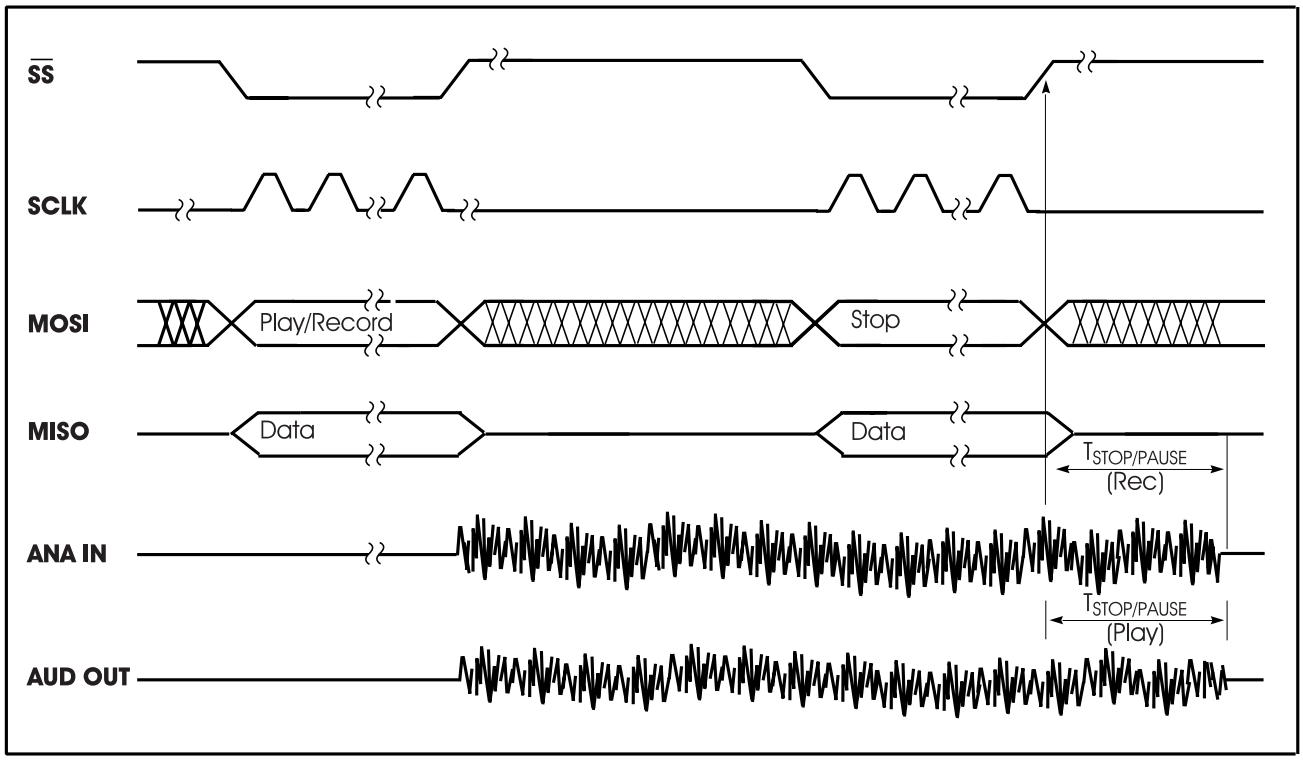
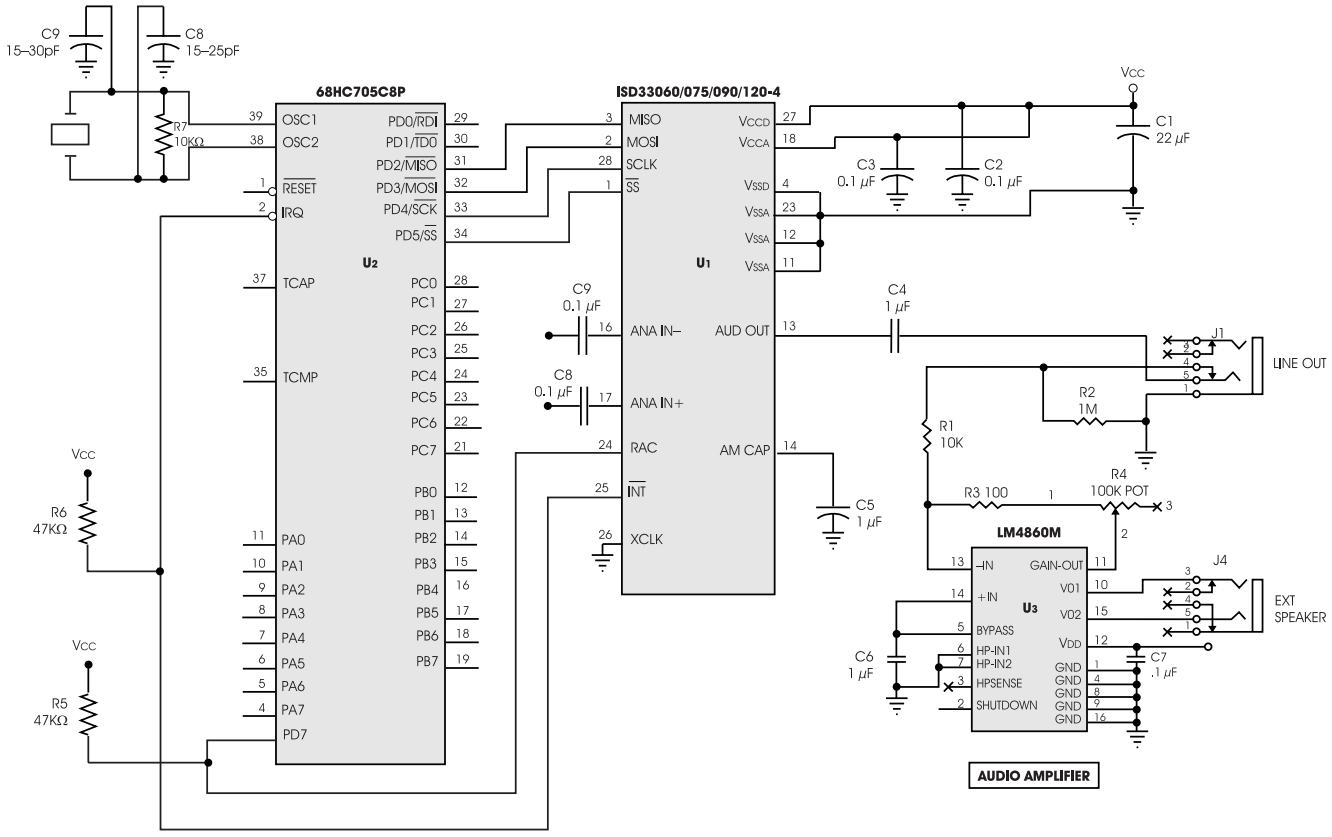
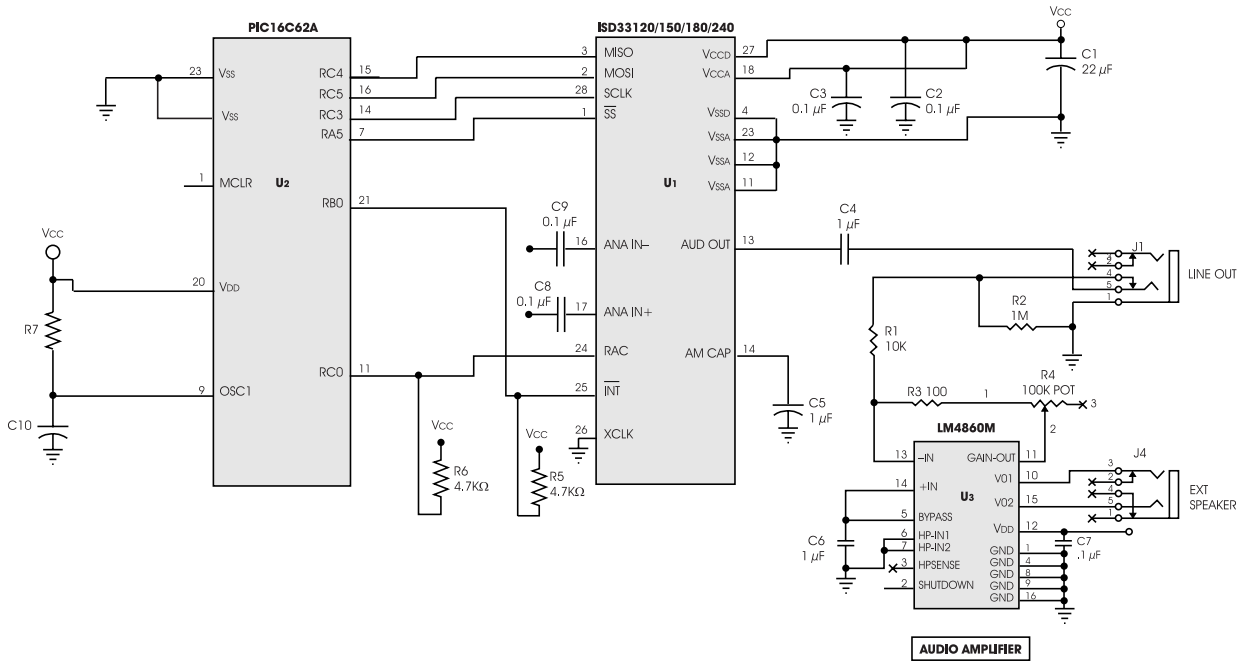


Figure 9: Application Example Using SPI



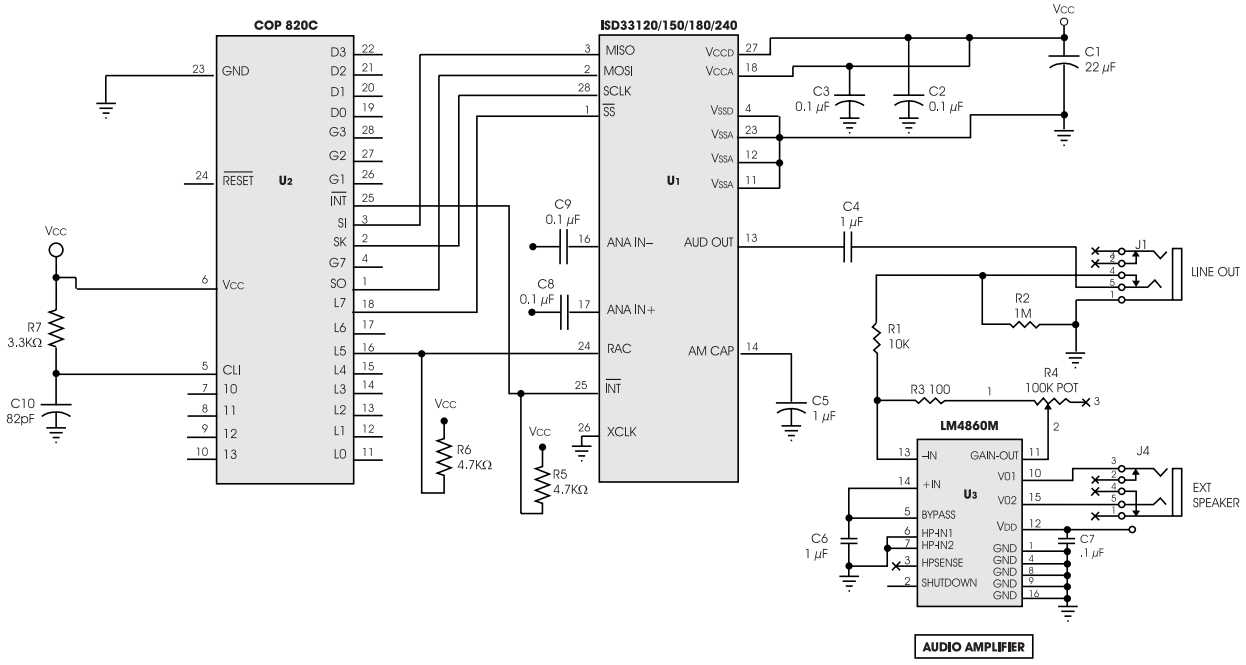
NOTE: *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*

Figure 10: Application Example Using Microwire



NOTE: *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*

Figure 11: Application Example Using SPI Port on Microcontroller



NOTE: *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*