IS24C16-3

16,384-BIT SERIAL ELECTRICALLY ERASABLE PROM

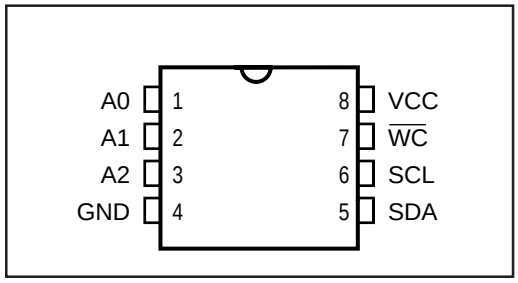
ADVANCE INFORMATION
JULY 1997

FEATURES

- Low power CMOS
  – Active current less than 3.0 mA
  – Standby current less than 35 µA
- Low voltage operation
  – Vcc = 2.7V to 5.5V
- 100 KHz Compatibility
- Hardware write protection
  – Write control pin
- Internally organized as eight banks
  – 256 pages x 8 bytes
- Two-wire serial interface
  — Bidirectional data transfer protocol
- Flexible byte write and 16-byte page-write modes
- High-reliability
  – Endurance: 100,000 cycles per byte
  – Data retention: 100 years
- Automatic word address incrementing
  — Sequential register read
- Filtered inputs for noise suppression
- 8-pin PDIP or SOIC packages

PIN CONFIGURATION

8-Pin DIP and SOIC



PIN DESCRIPTIONS

A0-A2	Address Inputs (No connection)
SDA	Serial Data I/O
SCL	Serial Clock Input
$\overline{WC}$	Write Control Input
Vcc	Power
GND	Ground

OVERVIEW

The IS24C16-3 is a low cost, low power, low voltage serial EEPROM and organized as 2,048 x 8 bits. The memory is configured as 128 pages of 16 bytes each. It is fabricated using *ISSI*'s advanced CMOS EEPROM technology and operates from a single supply.

The IS24C16-3 is internally organized as a 256 x 8 memory bank. The IS24C16-3 features a serial interface and software protocol allowing operation on a simple 2-wire bus. Included is a bidirectional serial data bus synchronized by a clock offering flexible byte write and a faster 16-byte page write. A write protect pin can protect data in the upper quadrant of memory.

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

A0, A1, and A2: These pins are not connected.

Write Control ($\overline{WC}$) - The Write Control input is used to disable any attempt to write to the memory. When HIGH, the upper quadrant of memory is protected against write operations; when LOW, the write function is normal. The part can be read independent of the state of $\overline{WC}$ pin. When not connected this pin will be pulled LOW.

GENERAL DESCRIPTION

The IS24C16-3 features a SERIAL communication, and supports bidirectional data transmission protocol allowing one IS24C16-3 operation on a simple two-wire bus. The two-wire bus is defined as a serial data line (SDA), and a serial clock line (SCL). (Refer to Figure 1. Typical System Bus Configuration.)

The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving device as a receiver. The device controlling the data transmission is named MASTER device, and the controlled device is named SLAVE device.

The IS24C16-3 does not use any device address bits but instead the three bits are used for memory page addressing. These page addressing bits should be considered the most significant bits of the data word address which follows. The A0, A1, and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is HIGH and a write operation is initiated if this bit is LOW.

The ACKnowledge is used to indicate successful data transfers. The transmitting device will release the data bus (SDA goes HIGH) after transmitting eight bits (one data bit is transfered at the falling edge of each clock cycle). During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge the transmitter that it received the eight bits of data. (Refer to Figure 2. ACKnowledge Response from Receiver Diagram.)

DEVICE OPERATION

START and STOP Conditions

Both SDA and SCL lines remain HIGH when the SDA bus is not busy. A HIGH-to-LOW transition of SDA line, while SCL is HIGH, is defined as the START condition. A LOW-to-High transition of SDA line, while SCL is HIGH, is defined as the STOP condition. (Refer to Figure 3. Start and Stop Conditions.)

Data Validity Protocol

One data bit is transferred during each clock cycle. The data on the SDA line must remain stable during the HIGH period of the clock cycle, because changes on SDA line during the SCL HIGH period will be interpreted as START or STOP control signals. (Refer to Figure 4. Data Validity Protocol.)

Device Addressing Byte Definitions

The most significant four bits of Device Addressing Byte (Bit 7 to Bit 4) are defined as the device type identifier. For IS24C16-3, this is fixed as 1010. The next three significant address bits (Bit 3 to Bit 1) are address memory bits. One IS24C16-3 device can be connected on the bus. The last bit Bit 0 defines the write or read operation to be performed. When set to “1”, a READ operation is selected; when set to “0” a WRITE operation is selected. (Refer to Figure 5. Device Addressing Byte Definitions.)

WRITE OPERATION

Byte Write

For a WRITE operation, the IS24C16-3 requires another 8-bit data word address following the Device Addressing Byte and ACKnowledgement. This data word address provides access to any one of the 256 data words of device's memory array.

Upon receipt of the data word address, the IS24C16-3 responds with an ACKnowledge on SDA, and waits for the next 8-bit data word, then again responding with an ACKnowledge. The master device terminates the Byte Write Operation by generating a STOP condition, afterward the IS24C16-3 begins the internal WRITE cycle to the nonvolatile memory array. Refer to Write Cycle Timing. All inputs are disabled during this write cycle and the device will not response to any requests from the master. (Refer to Figure 6. Write Operation for the Address, ACKnowledge, and Data Transfer Sequence.)

Page Write

The IS24C16-3 is capable of 8-byte page- WRITE operation. A page-WRITE is initiated in the same manner as a byte write, but instead of terminating the internal write cycle after the first data word is transfered, the master device can transmit up to 15 more words. After the receipt of each data word, the IS24C16-3 responds immediately with an ACKnowledge on SDA line, and the four lower order data word address bits are internally incremented by one while the four higher order bits of the data word address remain constant. If the master device should transmit more than 8 words, prior to issuing the STOP condition, the address counter will “roll over,” and the previously written data will be overwritten. All inputs are disabled until completion of the internal WRITE cycle. (Refer to Figure 7. Write Operation for the Address, ACKnowledge, and Data Transfer Sequence.)

Acknowledge Polling
Once the internal write cycle has started and the IS24C16-3 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the Device Addressing Byte. The read/write bit is representive of the operation desired. Only if the internal write cycle has been completed will the IS24C16-3 respond with an acknowledge on the SDA bus allowing the read or write sequence to continue.

READ OPERATION

READ operations are initiated in the same manner as WRITE operations, except that the read/write bit of the device addressing byte is set to "1". There are three READ operation options: current address read, random address read and sequential read.

Current Address Read
The IS24C16-3 contains an internal address counter which maintains the address of the last data word accessed, incremented by one. For example, if the previous operation either a read or write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the IS24C16-3 receives the Device Addressing Byte with a READ operation (read/write bit set to "1"), it will respond an ACKnowledge and transmit the 8-bit data word stored at address location n+1. If the Current Address READ operation only accesses a single byte of data, the master device terminates the Current Address READ operation by pulling ACKnowledge HIGH (lack of ACKnowledge) indicating the last data word to be read, followed by a STOP condition. (Refer to Figure 8. Current Address Read Diagram.)

Random Access Read
Random Address READ operation allows the master device to access any memory location in a random fashion. This operation involves a two-step process. First, the master device generates a START condition and initiates Device Addressing Byte with a WRITE operation (read/write bit sets to "0"), followed by the address of the data word the master device is to READ. This procedure stores the desired address of data word to the internal address counter of the IS24C16-3.

After the data word address ACKnowledge is received by the master device, the master device now initiates a *CURRENT ADDRESS READ* by sending Device Addressing Byte with a READ operation (read/write bit sets to "1"). The IS24C16-3 responds with an ACKnowledge and transmits the eight data bits stored at the address location where the master device is to READ. At this point, the master device terminates the operation by pulling ACKnowledge HIGH (lack of ACKnowledge) indicating the last data word to be read, followed by a STOP condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read
Sequential Reads can be initiated as either a Current Address Read or Random Address Read. The first data word is transmitted as with the other byte read modes, the master device now responds with an ACKnowledge indicating that it requires additional data from the IS24C16-3. The IS24C16-3 continues to output data for each ACKnowledge received. the master device terminates the sequential READ operation by pulling ACKnowledge HIGH (lack of ACKnowledge) indicating the last data word to be read, followed by a STOP condition.

The data output is sequential, with the data from address n followed by the date from address n+1, ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential read operation. When the memory address boundry (address 255) is reached, the address counter "rolls over" to address 0, and the IS24C16-3 continues to output data for each ACKnowledge received. (Refer to Figure 910. Sequential Read Operation Starting with a Random Address READ Diagram.)

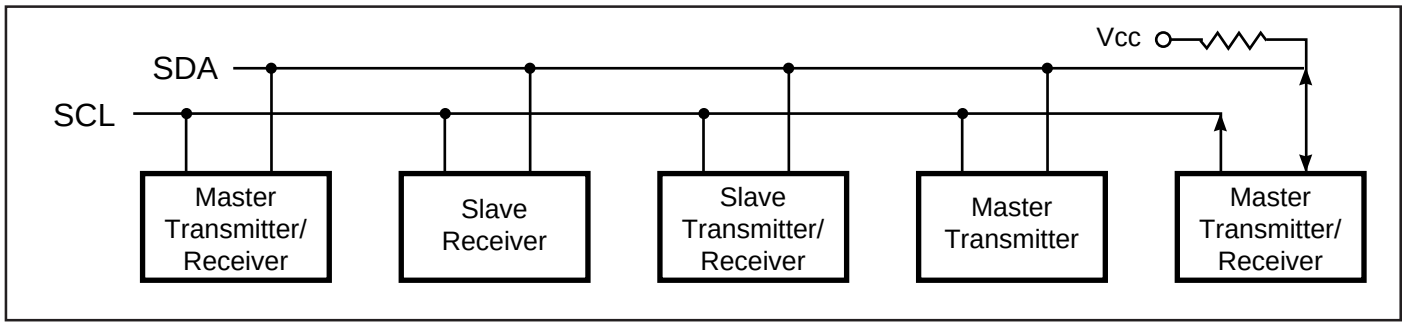


Figure 1. Typical System Bus Configuration

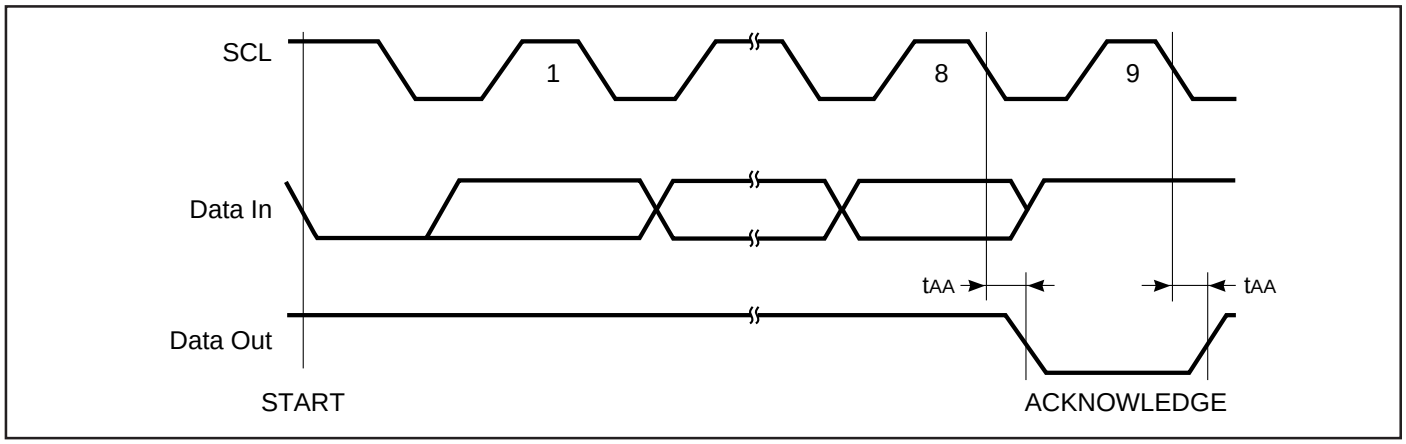


Figure 2. Output Acknowledge

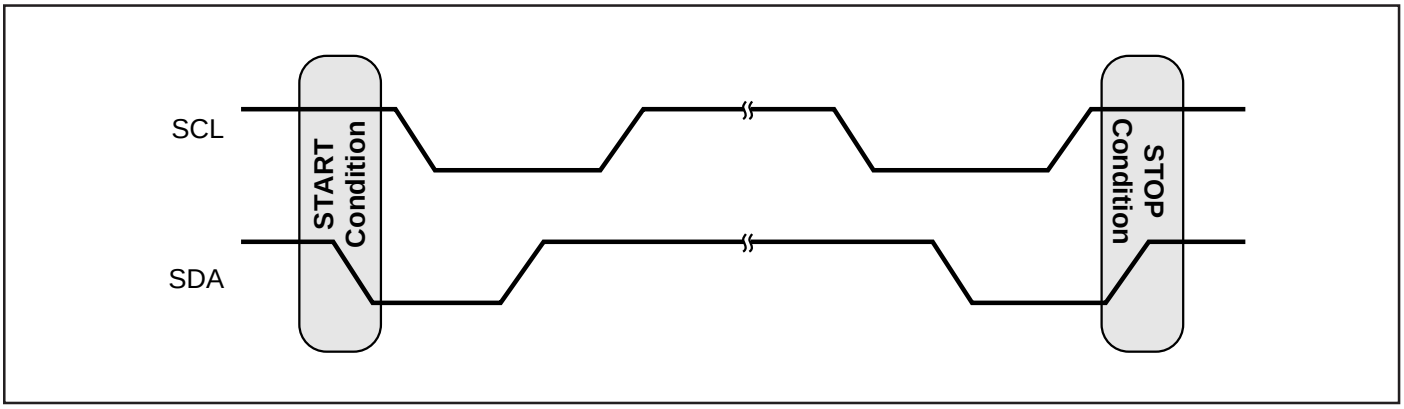


Figure 3. START and STOP Conditions

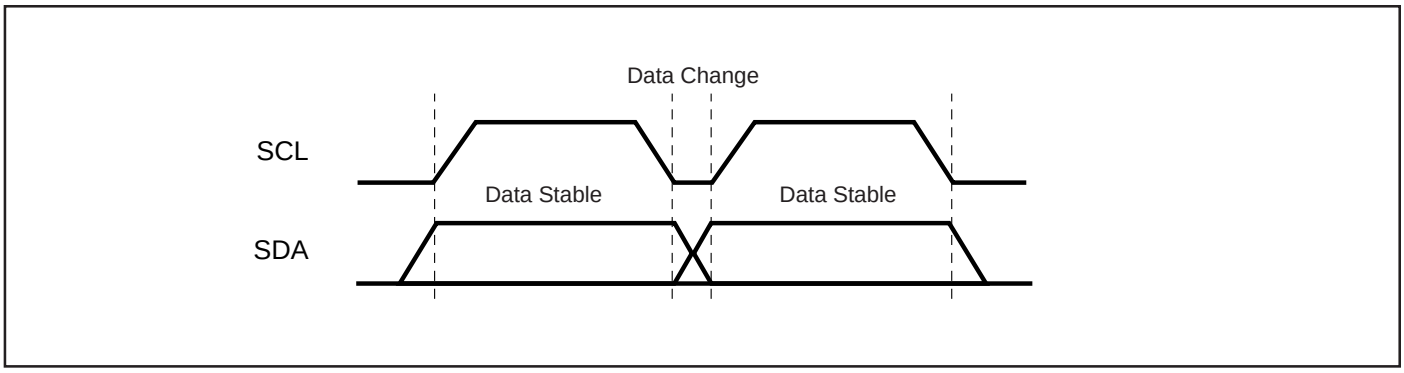


Figure 4. Data Validity Protocol

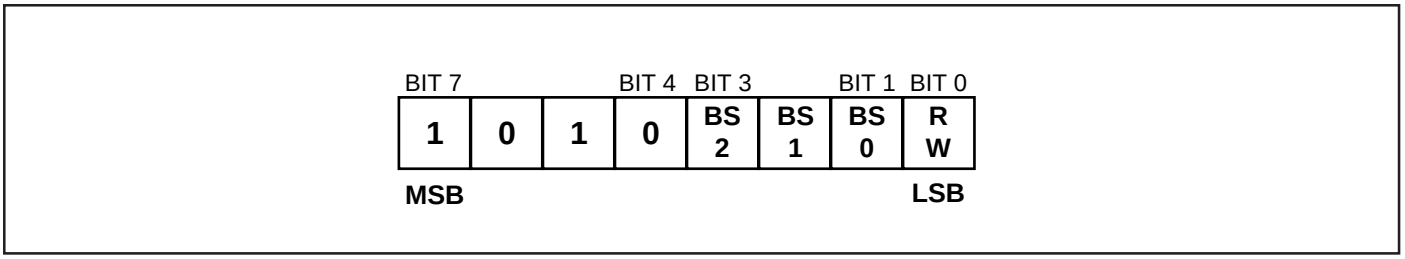


Figure 5. Device Addressing

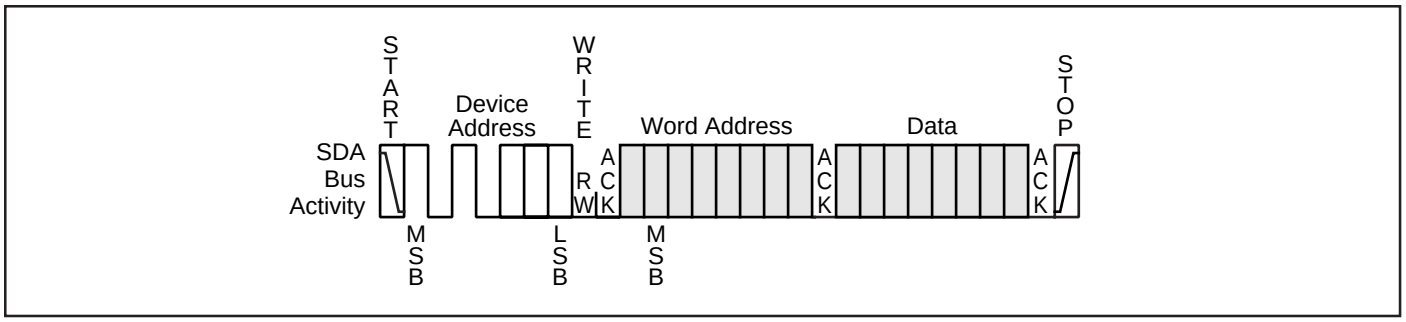


Figure 6. Byte Write

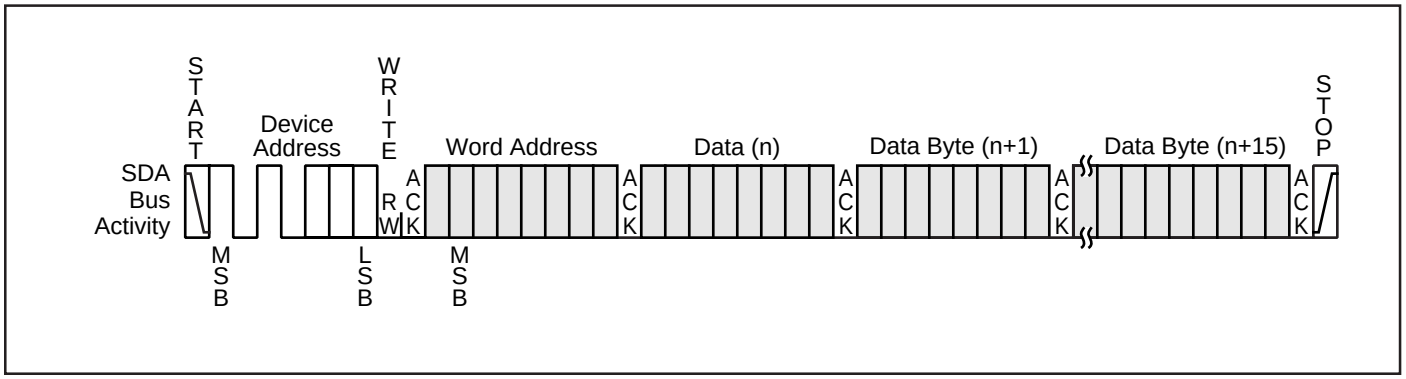


Figure 7. Page Write

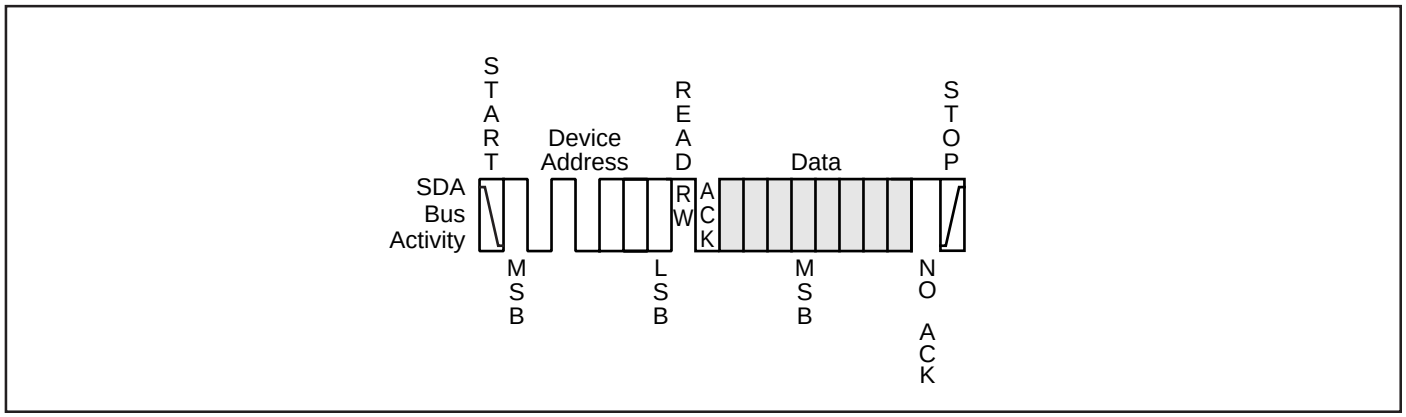


Figure 8. Current Access Read

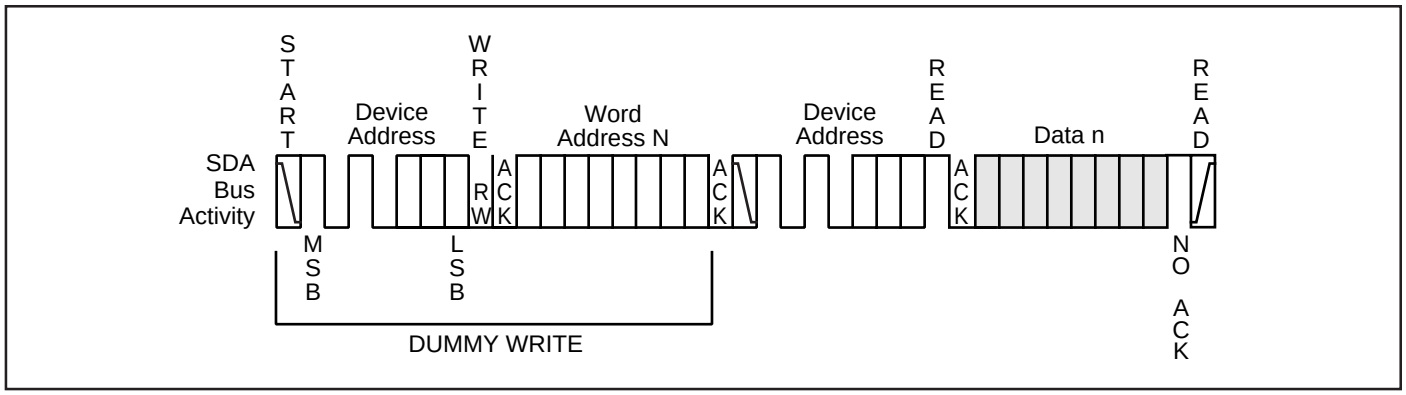


Figure 9. Random Access Read

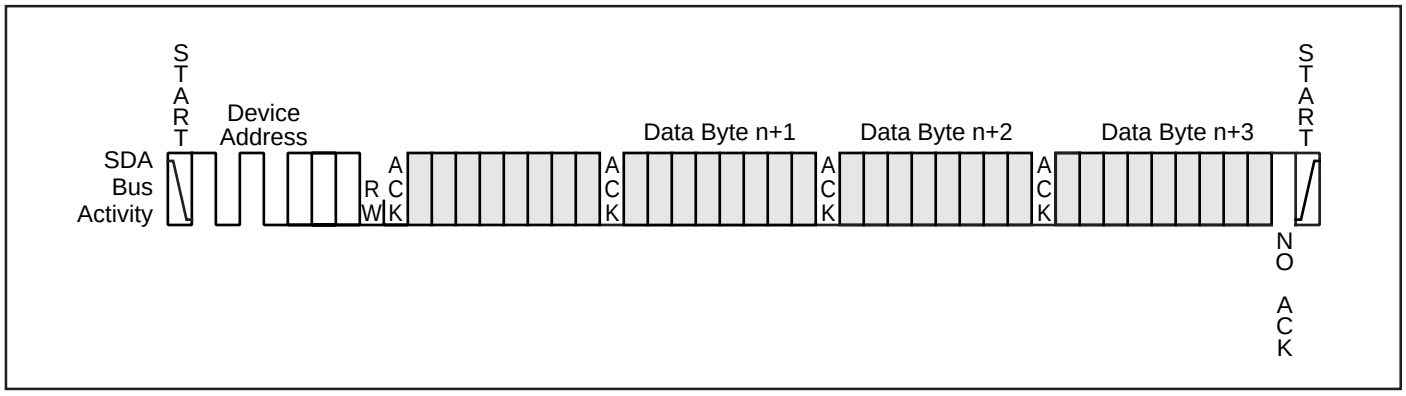


Figure 10. Sequential Read

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	0.5 to +7.0	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V to 5.5V
Industrial	–40°C to +85°C	2.7V to 5.5V

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for IS24C16-3 and –40°C to +85°C for IS24C16-3I, Vcc = 2.7V to 5.5V.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL1}	Output LOW Voltage	V_{CC} = 2.7V., I_{OL} = 0.15 mA	—	0.25	V
V_{OL2}	Output LOW Voltage	V_{CC} = 3.0V., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		—	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–1.0	—	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} max.	—	3	µA
I_{LO}	Output Leakage Current		—	3	µA

POWER SUPPLY CHARACTERISTICS

T_A = 0°C to +70°C for IS24C16-3 and –40°C to +85°C for IS24C16-3I, Vcc = 2.7V to 5.5V.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Current	READ at 100 KHz	—	1.0	mA
I_{CC2}	Vcc Operating Current	WRITE at 100 KHz	—	3.0	mA
I_{SB1}	Standby Current	Vcc = 2.7V	—	4.0	µA
I_{SB2}	Standby Current	Vcc = 5.5V	—	35.0	µA

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for IS24C16-3 and –40°C to +85°C for IS24C16-3I, Vcc = 2.7V to 5.5V

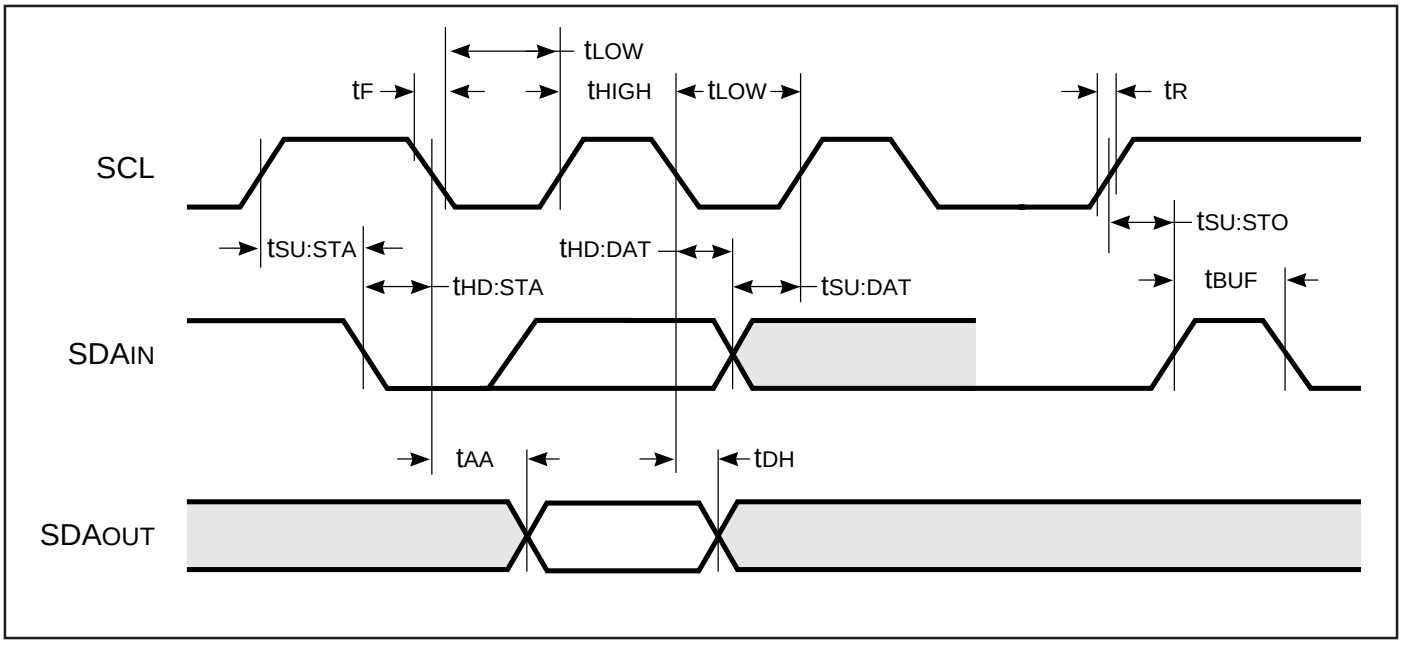
Symbol	Parameter	Test Conditions	2.7V Min.	2.7V Max.	5V Min.	5V Max.	Unit
f_{SCL}	SCL Clock Frequency		0	100	0	400	KHz
T	Noise Suppression Time		—	100	—	50	ns
t_{LOW}	Clock LOW Period		4.7	—	1.2	—	µs
t_{HIGH}	Clock HIGH Period		4	—	0.6	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)		4.7	—	1.2	—	µs
$t_{SU:STA}$	Start Condition Setup Time		4.7	—	0.6	—	µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7	—	0.6	—	µs
$t_{HD:STA}$	Start Condition Hold Time		4	—	0.6	—	µs
$t_{HD:STO}$	Stop Condition Hold Time		4	—	0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time		200	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time		0	—	0	—	ns
t_{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	100	—	50	—	ns
t_{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	4.5	0.1	0.9	µs
t_R	SCL and SDA Rise Time(1)		—	1000	—	300	ns
t_F	SCL and SDA Fall Time(1)		—	300	—	300	ns
t_{WR}	Write Cycle Time		—	10	—	10	ms

Note:

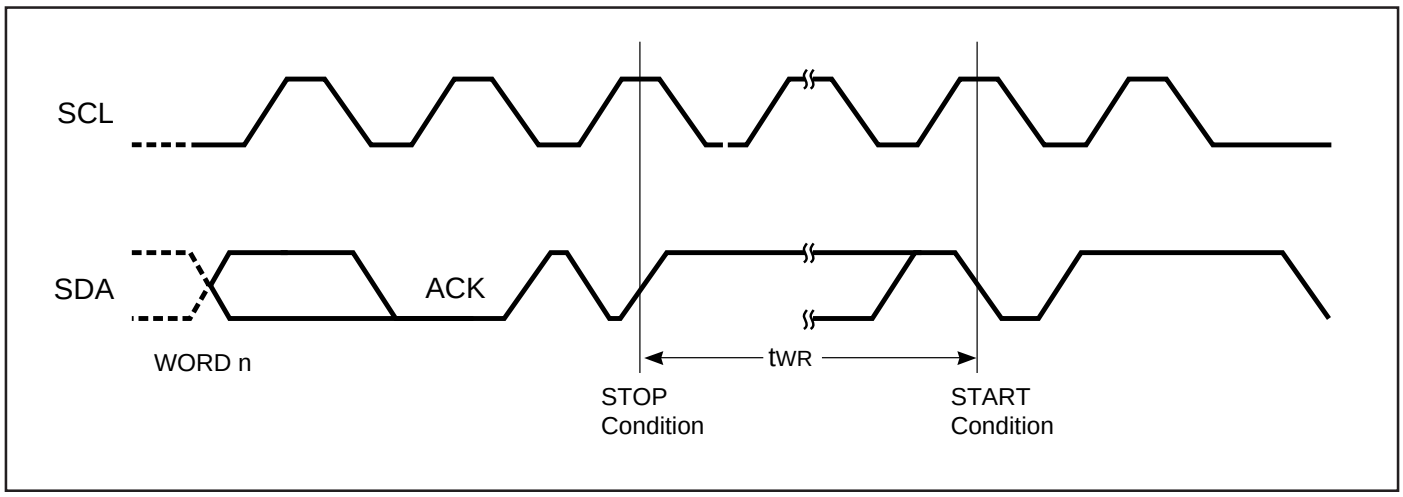
1. This parameter is characterized but not 100% tested.

AC WAVEFORMS

BUS TIMING



WRITE CYCLE



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
100 KHz	IS24C16-3P	300-mil Plastic DIP
100 KHz	IS24C16-3G	Small Outline (JEDEC STD)

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Frequency	Order Part Number	Package
100 KHz	IS24C16-3PI	300-mil Plastic DIP
100 KHz	IS24C16-3GI	Small Outline (JEDEC STD)

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Fax: (408) 588-0806
Toll Free: 1-800-379-4774
e-mail: sales@issiusa.com
http://www.issiusa.com